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Fast-tuning VCOs with digital tuning and PROM correction will compete with YIG oscillators for wide band, high linearity applications. Watkins-Johnson's entry in the field is described in the Cover Story beginning on p. 131. Cover design by Owen Finstad, Art Director, Watkins-Johnson Co.

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Microwave Switching With GaAs FETs

Device and Circuit Design Theory and Applications

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Introduction

There is a growing need for high-performance, small, versatile, and inexpensive microwave switches in phased-array systems and electronic warfare applications. The use of GaAs FETs as switch elements to help meet these needs has been reported recently in various microwave applications[1-7]. These switches have already been demonstrated to provide subnanosecond switching speeds, multiwatt power-handling capability, virtually zero control power dissipation, and compatibility with monolithic applications.

This article discusses the design considerations for a switch FET, theoretical determination of its equivalent circuit under switching conditions, rf and dc circuit design requirements, and large-signal operation considerations for power switching applications. Design examples and experimental data from monolithic TR switches, phase shifters, and high-power switches will be given.

GaAs FET as a Switch

The FET switch is a three-terminal device with the gate voltage V_g controlling the switch states. In a typical switch mode, the high impedance state corresponds to a negative gate bias larger in magnitude than the pinchoff voltage ($|V_g| > |V_p|$), and the low impedance state corresponds to zero gate bias. These two linear operation regions of the FET are shown schematically in Figure 1.

Note that in either state virtually no dc bias power is required. Therefore the switches can practically be classified as passive as far as the overall power consumption is concerned: this leads to enor-

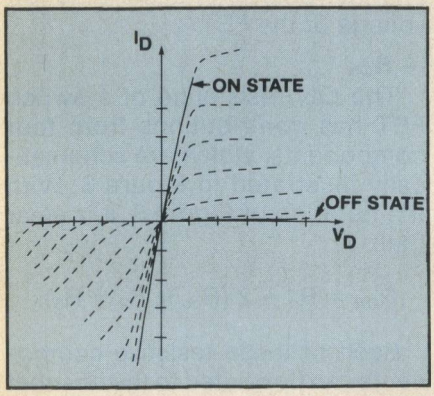

Fig. 1 Two linear operation regions of an FET switch.

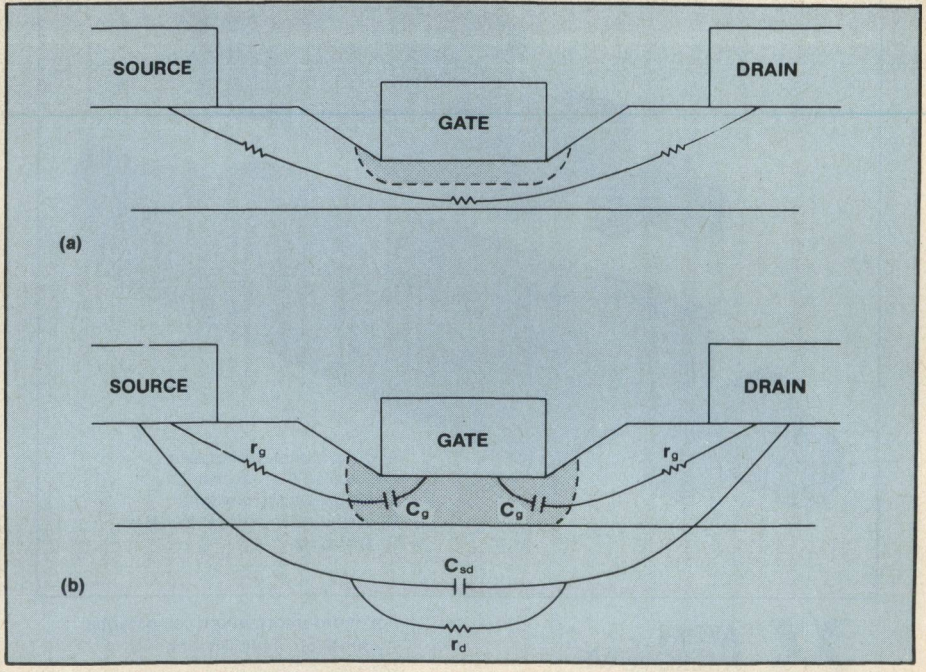

Fig. 2 Schematic cross-section of an FET showing various resistive and capacitive regions. a) No gate bias b) $|V_g| > |V_p|$.

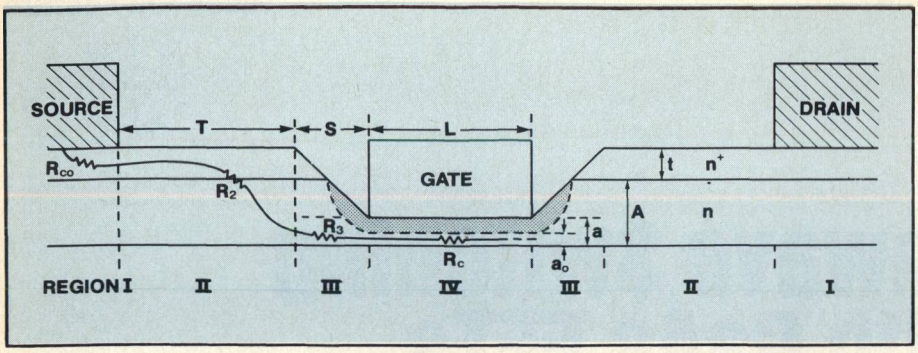

Fig. 3 Schematic cross-section of an FET showing various resistive sections contributing to the R_{ON} of the switch.

mous simplifications in driver requirements. Although the FET itself is a three-terminal device, the switch is bidirectional.

The cross-section of a simple FET structure appears in Figure 2. When no gate bias is applied, the channel is open except for the zero field depletion layer thickness. Hence, for current levels less than the saturated channel current I_{dss}, the FET can be modeled as a linear resistor.

When a negative gate voltage V_g is applied between gate and source so that $|V_g| > |V_{pinchoff}|$, the channel can be completely depleted of free charge carriers. Under this bias condition, the FET can be modeled by series and parallel combination of resistors and capacitors. The approximate region of the FET responsible for each element is shown in Figure 2b.

Assuming that the gate termination represents a high rf impedance at the frequency of operation, the OFF-state equivalent circuit can be expressed as a parallel combination of a resistor and a capacitor. For $1/\omega C_g >> r_g$, the effective drain-to-source capacitor is simply $(C_{sd} + C_g/2)$ and the effective drain resistor is the parallel combination of R_d and $2/(\omega^2 C_g^2 r_g)$. The figure of merit for a switch FET can simply be expressed as the ratio of its effective OFF state resistance to its ON resistance.

Design Consideration for a Switch FET

Let us examine the effect of various device parameters on the device equivalent circuit. The important parameters are the channel geometry, gate length, the channel doping and the pinchoff voltage of the FET.

— R_{ON}

The ON resistance of a switch FET has contributions from four components, which are schematically illustrated in Figure 3. With the notation of Figure 3, it is clear that:

$$R_{ON} = R_c + 2\,(R_{co} + R_2 + R_3).$$

Each of these resistive components can be related to the channel parameters of the FET. Let us examine each one separately.

R_{co}: The constant resistance R_{co} can be calculated as[8]:

$$R_{co} = \frac{2.1}{W\, t\, n_+^{0.66}}\ \Omega$$

where W is the gate periphery in mm, t the thickness of the n_+ region under the source contact in μm. n_+ is the doping density of the contact layer expressed in units of 10^{16} cm^{-3}.

R_2: To estimate the value of R_2, region II can be modeled in terms of incremental resistances, as shown in Figure 4.

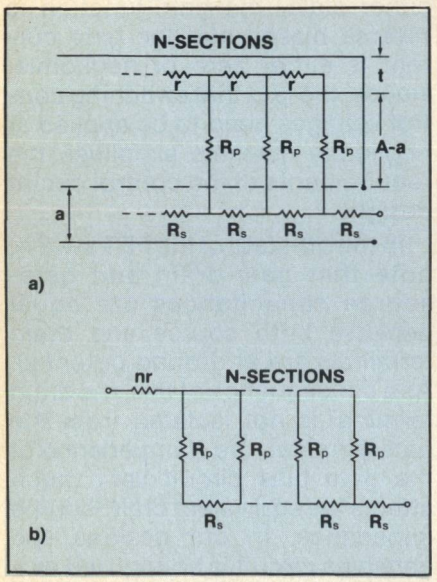

Fig. 4 Equivalent incremental resistance circuit for calculating the contribution of Region II. a) actual resistance distribution b) approximate resistance distribution for $R_s >> r$.

However, to obtain a simple formula, we can use the circuit model in Figure 4 when $R_s >> r$. Making an analysis similar to Berger[9], and using Fukui's formula for the resistivity of GaAs[8], the resistance R_2 can be expressed in a closed-form equation as:

$$R_1 = \frac{1.1\, T}{W\, t\, n_+^{.82}} + \frac{1.1}{w\, n^{.82}} \left(\frac{A-a}{a}\right)^{0.5} \Omega\ .$$

In this paper, all the doping levels are in units of 10^{16} cm^{-3}, and all the lengths are expressed in μm except the gate periphery W, which is in mm.

R_3: This is the contribution of the bevelled section. Here it is difficult to define the current paths with any accuracy. We will assume that the conduction region is confined to a region of height a and length S. If we further assume that the slope of the bevel is 45°, then S = t + A-a. Hence, R_3 becomes:

$$R_3 = \frac{1.1\,(t + A - a)}{W\, a\, n^{.82}}\ \Omega\ .$$

R_c: The open channel resistance can be estimated as[8]:

$$R_c = \frac{1.1\, L}{W\, a_o\, n^{.82}}\ \Omega\ .$$

In this equation, a_o is the fraction of the channel which is open. For GaAs FETs with a given pinchoff voltage V_p and channel doping, it can be calculated as:

$$a_o = \frac{.378}{n^{0.5}}\,(V_p + 0.85)^{0.5} - (0.85)^{0.5}$$

The channel resistance calculated through the equations above is typically a lower limit to what one observes experimentally. This could be due to the proximity of the interface between the channel and buffer layer, which makes it difficult to precisely define either the mobility or the doping level under the gate.

TABLE I

CALCULATION OF EQUIVALENT CIRCUIT PARAMETERS FOR A TYPICAL 1 MM GaAs FET SWITCH

Design Parameters	Equivalent Circuit Parameters
W = 1 mm	R_{ON} = 2.7 Ω
L = 1 μ	C_{sd} = 0.14 pF
V_p = -4 V	R_{OFF} = 3 K Ω
n = 10^{17} cm^{-3}	R_g = 1.4 Ω
n^+ = 2 x 10^{18} cm^{-3}	C_g = 0.22 pF
A = .37 μm	
T = 2 μm	
S = 0.3 μm	
t = 0.2 μm	
a_o = 0.15 μm	
a = 0.26 μm	

— OFF-State Equivalent Circuit Parameters

C_{sd}: The source-drain capacitance C_{sd} represents the fringing capacitance between the source and drain electrodes.

A good estimate of these capacitances can be obtained by considering the electrostatic coupling between two parallel conductors on a surface of a semi-infinite dielectric medium, representing the GaAs chip. Using this model, the capacitance expression becomes[10]:

$$C_{sd} = (\varepsilon_r + 1)\,\varepsilon_o\, W\, \frac{K\,(1-k^2)^{1/2}}{K\,(k)}$$

where K (k) is the complete elliptic integral of the first kind. The argument k is related to the geometry of electrodes as:

$$k = \left[\frac{(2L_s + L_{sd})\, L_{sd}}{(L_s + L_{sd})^2}\right]^{1/2}$$

where L_{sd} is the interelectrode spacing between the drain and source electrodes. In these expressions, it is assumed that $L_s = L_d$ and $L_s >> L_{sd}$.

Source-drain capacitance is typically in the 0.14 pF range for 1 mm FETs and it is independent of device parameters such as channel doping and pinchoff voltage.

r_d: The resistor in parallel with C_{sd} represents the rf losses associated with C_{sd}. Our experience indicates that 3 K Ω for 1 mm gate devices representing a Q of around 25 at X-band frequencies is a reasonable choice.

C_g: C_g represents the drain-to-gate and gate-to-source capacitances. These capacitances are equal because of symmetry. If there is a gate pad of significant area, its capacitance to ground needs to be added to the equivalent circuit.

There is no precise way of estimating C_g. A simple-minded approach that gives C_g values in good agreement with experimental results is to use half the gate capacitance with the channel fully depleted so that:

$$C_g = 0.06\, \frac{WL}{a}\ \text{pF}\ .$$

Note that a is related to both channel doping and the pinchoff voltage of the device.

[Continued on page 64]

r_g: The resistor r_g represents the changing resistance of C_g. Again, we do not know a precise way of calculating this resistance. Experimental evidence suggests that one-half of R_{ON} is a reasonable value for r_g.

In the light of the discussion above, we can estimate the equivalent circuit of a typical GaAs switch FET. Table 1 summarizes typical channel parameters for a 1 mm total gate periphery, 1 μm gate length FET with -4 V pinchoff voltage and 10^{17} cm^{-3} channel doping.

These equivalent circuit values translate to equivalent off-to-on resistance ratios of 800 at 10 GHz. This ratio decreases to 420 at 20 GHz, which is probably the end of the useful range for 1 μm gate length switch FETs. To push the operating frequency to higher frequencies, one needs to go to submicron gate lengths to decrease C_g and R_{ON} and thus increase the switching equivalent resistance ratio.

We can also estimate the switching speed from the equivalent circuit. Assuming that the gate bias circuit is fed at 50 ohms impedance level and a total of 6 pFs are used in the bias circuit low pass filter, one reaches the conclusion that charging time constants are in the 0.3 nsec range. Experimental evidence also indicates that switching times of 1 nsec are quite possible, as shown in Figure 5. By optimizing the gate bias circuit design, switching times which are significantly smaller than 1 nsec are feasible.

Circuit Design Considerations

Switching circuits with FETs can be designed in essentially the same way as PIN diodes; this is done using on and off state equivalent circuits as required in the overall circuit configuration.

Although in this article we will discuss the monolithic circuit applications of switching FETs, it should be pointed out that it is quite possible also to use discrete FETs in hybrid form. Similar to PIN diodes, the FETs can be in series or shunt mode with respect to the transmission lines. There are, however, some salient features of FET switch circuit design that need to be mentioned.

The FET is a three-terminal device; the switching occurs only through the gate control voltages and no other bias is required for the operation of the phase shifter. The rf transmission lines do not carry any dc voltage and therefore there is no need for dc blocking capacitors between various switch elements: a significant design advantage.

Gate control voltages corresponding to the two switch states are $V_{g1} = OV$ and $V_{g2} = -V$ where $V > V_p$. In either state, the gate junction is reverse biased and the gate current is either zero or negligible. Hence, the fact that switching control voltages need to be applied at negligible currents simplifies the requirements of the control circuit design.

In the off-state of the FET switch, note that gate-drain and gate-source capacitances are equal because both source and drain terminals are at ground potential. As a consequence of this, the drain terminal is not isolated from the gate terminal: the rf impedance of the gate bias circuit very much affects the equivalent drain-source impedance. In our designs, the gate bias circuit is configured as a two-section low pass filter providing an effective rf open to the FET at the gate terminal. When gate terminating impedance is very high, the equivalent drain-source capacitance can simply be approximated as $C_d + C_g/2$.

Note that the total drain capacitance shunting r_d represents a reactance of the order of 50 ohms at X-band frequencies. Therefore, to realize the switching action, this capacitance must be either resonated or its effect must be included in the design of the impedance matching sections. This is an important design consideration for FET switches, as it directly relates to the operation bandwidth.

Tuning out the effective drain-source capacitance can simply be accomplished by connecting an inductive reactance between the drain and source terminals. Monolithic circuit technology also allows distributing the switch FET and its associated drain capacitance along

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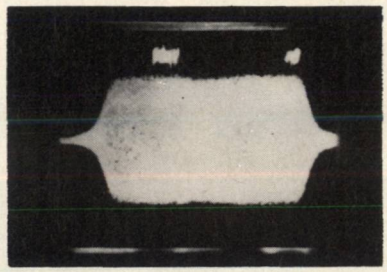
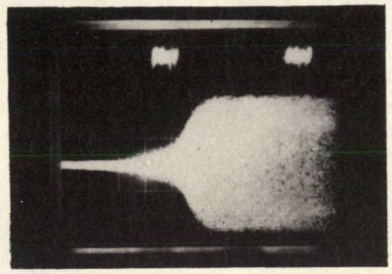
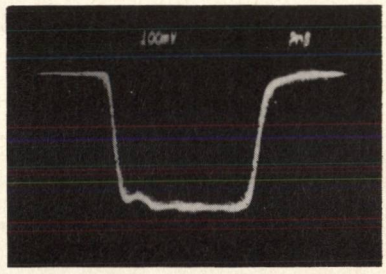


RF FREQUENCY 10 GHZ
RF OUTPUT 0 DBM
HORIZONTAL 1 NANOSECOND/DIVISION



HORIZONTAL
500 PICOSECONDS/DIVISION



SWITCH CONTROL SIGNAL
HORIZONTAL: 2 ns/DIV
VERTICAL: 1 V/DIV

Fig. 5 Monolithic TR switch switching data.

a transmission line structure. Consider the distributed switch approach shown in Figure 6[5]. In this structure, the drain-source capacitance and the overlay inductance are treated as the per-unit-length capacitance and per-unit-length inductance of an artificial transmission line. The source pad is grounded by a via hole.

The configuration shown in Figure 6 has two major design advantages: First, by integrating the FET into the rf transmission line, the intrinsic switch element of the FET is placed at the point where it is most effective. This eliminates the contribution of undesirable FET parasitic elements such as the drain pad capacitance and the extra transmission line sections that would have been required to connect a discrete FET to the rf line. Second, by including the effect of the overlay inductance itself or by adding extra inductive elements between sections, the drain-source capacitance of the FET in the high impedance state can be effectively tuned out over a wider frequency range. When wide frequency band operation of FET switches is required, the distributed switch FET approach provides the solution.

Figure 7 shows the chip picture of an X-band monolithic transmit/receive switch[3]. The FETs have an interdigital structure with sixteen 100 μm wide channels. If two single-gate cells sharing a single drain finger are considered to be a unit cell, then there are eight unit cells connected by an overlay structure to form a lumped element transmission line. Because in this circuit the overlay inductance is small, it compensates only a fraction of the drain capacitance. The U-shaped shorted stub acts as the main tuning element. The experimental results for the switch indicate a 1 dB insertion loss bandwidth of 8-12 GHz with minimum insertion loss around 0.5 dB. Isolation between the transmit and receive arms is better than 30 dB across the band. The chip dimensions are 3 x 3 x 0.1 mm.

For microwave power switching using FETs, there are additional considerations. One of these considerations is the maximum allowable rf voltage swing across the device. The variation of the rf voltage on the drain and gate terminals with respect to the grounded source is shown in Figure 8 for one period[7].

In this figure, it is assumed that the gate terminal of the switch FET is rf open. This condition should be realized in the design of the gate bias circuitry.

Under the above assumption and because gate-to-drain impedance and gate-to-source impedance are equal, half of the drain voltage swing appears in the gate terminal, as illustrated in Figure 8. Constraints on the terminal voltages can be summarized as follows. During the first half of the period, the total gate voltage should not fall below the pinchoff voltage V_p. During the entire cycle, the difference between the drain and gate

[Continued on page 68]

[From page 66] **MICROWAVE SWITCHING**

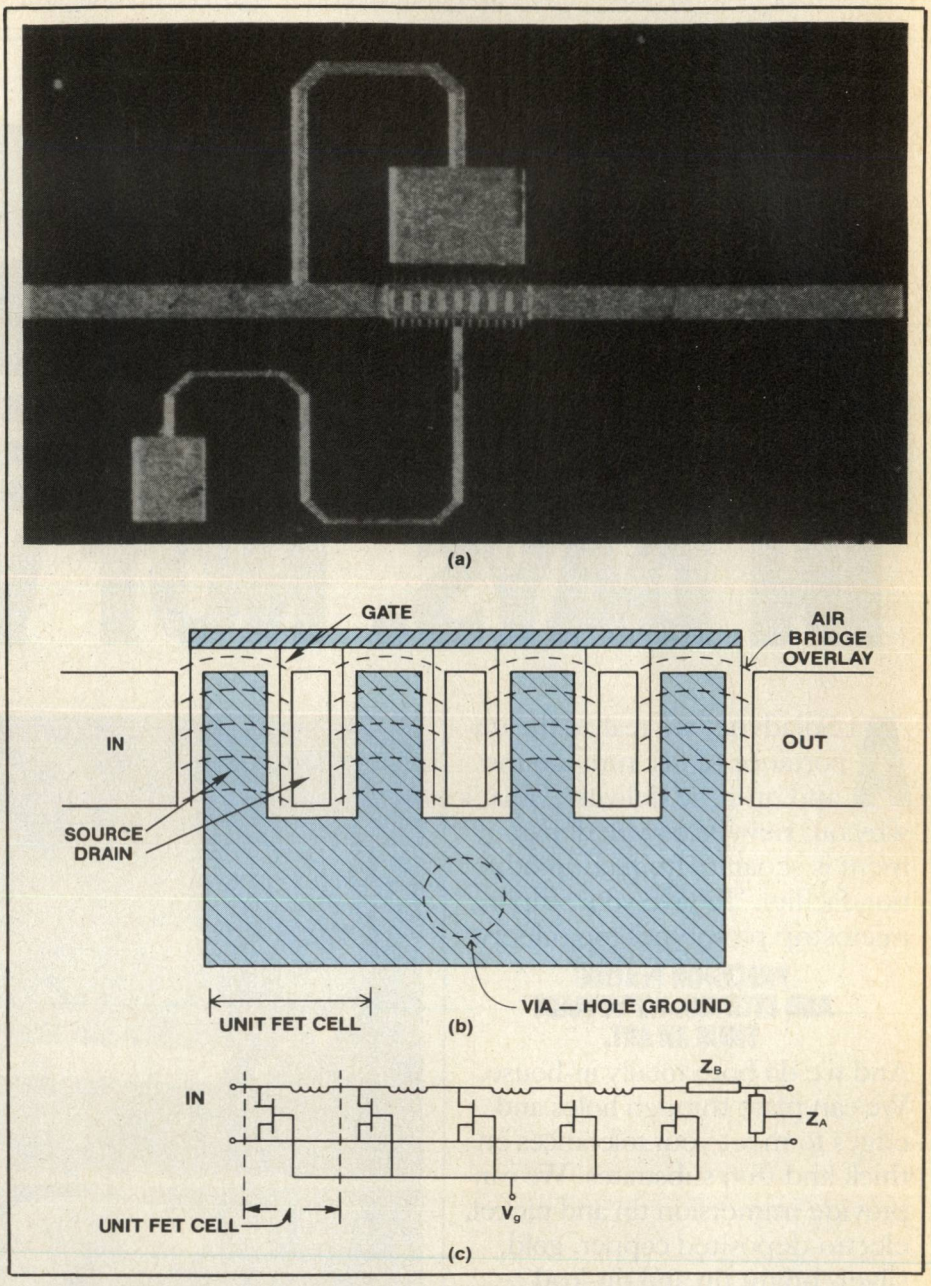


Fig. 6 Monolithic distributed switch approach. a) 1 × 1 switch in monolithic form b) FET structure c) equivalent circuit.

voltages should not exceed the gate-drain breakdown voltage. These contraints can be expressed mathematically as:

$$-V_{G_{bias}} + \frac{V_{Dmax}}{2} = -V_p$$

and

$$V_{Dmax} + V_{G_{bias}} - \frac{V_{Dmax}}{2} = V_B \ .$$

From these two equations, the maximum allowable drain voltage and the required gate bias condition can be solved as:

$$V_{Dmax} = V_B - V_p$$

and $$V_{G_{bias}} = \frac{V_B + V_p}{2} \ .$$

Hence, if the impedance level that the switch FET sees in its high impedance state is Z_o, then the maximum power that can be transmitted in the switch closed position can be calculated as:

$$P_{max} = \frac{1}{2} \frac{(V_B - V_p)^2}{Z_o} \ .$$

Using the notation of the schematic TR switch shown in Figure 9, Z_o can approximately be calculated by transferring the 50 ohm antenna terminal impedance through the

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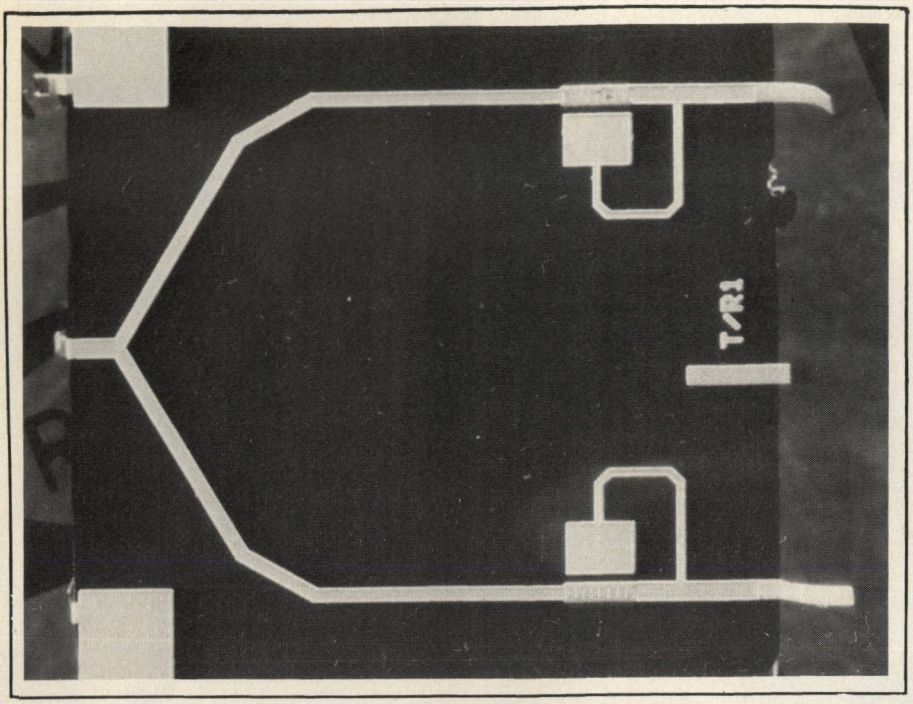

Fig. 7 X-band monolithic transmit/receive switch.

quarter wavelength MS line of characteristic impedance Z_1, as:

$$Z_o \simeq \frac{Z_1^2}{50} .$$

Hence,

$$P_{max} = 25 \frac{(V_B - V_p)^2}{Z_1^2} .$$

The maximum power calculation under switch closed condition is relevant to the transmitter arm of a transmit/receive (TR) switch. For the receiver arm, the constraints are different. During the time when the transmitter power is on, the switch on the receiver arm is in the open state. In this low impedance condition, it should be able to sustain essentially the short circuited current in the receive arm due to the transmitter pulse. Again using the notation of Figure 9, the peak

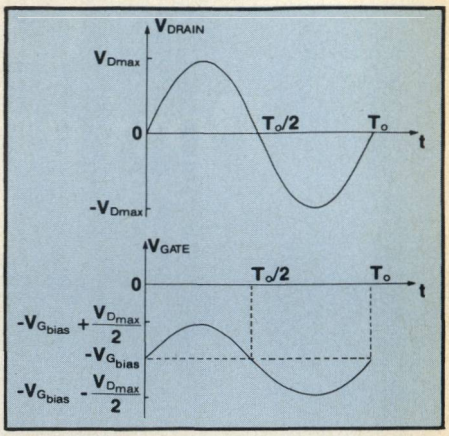

Fig. 8 Variation of the large signal rf voltages on drain and gate terminals over one period.

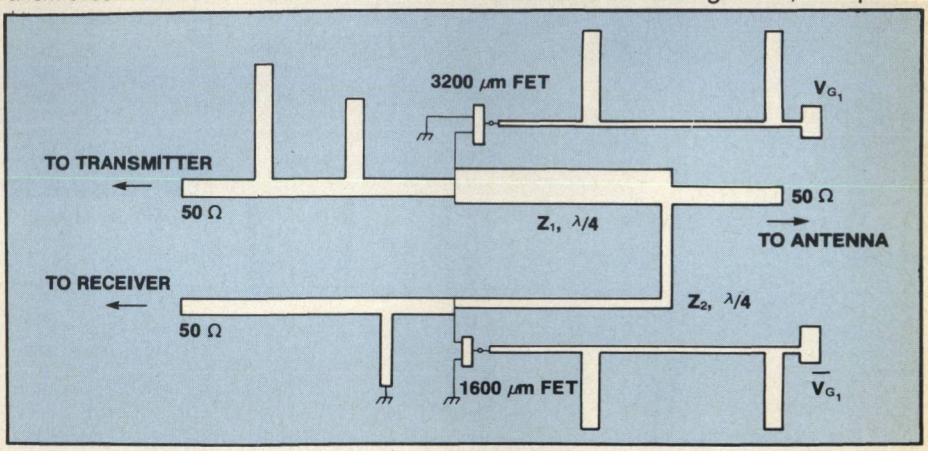

Fig. 9 The schematic circuit diagram of the 10 W transmit-receive switch.

value of this current can be calculated as:

$$I_{max}\ \text{switch open} = 20\sqrt{\frac{P_{Transmitted_{max}}}{Z_2\,(50 + Z_2)}}$$

Equations for P_{max} and I_{max} fully specify the constraints on the switch FETs under power-switching conditions. First note that constraints on the transmitter and the receiver arm switches are completely independent. Also note that in the equation for P_{max}, periphery of the device is not a parameter. Thus, once Z_1 is chosen from power requirements, the device periphery on the transmitter arm can be determined purely from small signal insertion loss analysis. On the other hand, the equation for I_{max} does bring in the device periphery as a design parameter for the receiver arm switch, since the maximum current that a device can support in its linear region before it reaches the saturation is directly proportional to its gate periphery. The characteristic impedance of the receiver arm, Z_2, also enters into the equation. It is easy to see that, by increasing Z_2, one can meet the requirement for I_{max} readily.

The switch described in Figure 9 is fabricated on 0.1 mm GaAs substrate[7]. A photograph of the finished chip is shown in Figure 10. The chip dimensions are 4.5 x 3.7 mm. In the transmit arm, a single-gate, interdigitated 3.2 mm total gate periphery FET is used. The receive arm uses a single-gate FET of 1.6 mm total periphery.

The dc gate circuitry is provided monolithically on-chip. It is essentially a low pass filter which provides high impedance to the gate of the device and isolates the bias pad at the edge of the chip from rf leakage, at X-band frequencies.

The experimental data indicates insertion losses in the 0.8-1.6 dB range with higher than 25 dB isolation. No degradation from small signal performance is observed up to 10 W of CW microwave power[7].

The FET switches, with their fast switching times and negligible dc power consumption, are ideal for passive phase-shifting circuits. As an example for this application, consider the X-band four-bit phase shifter chip shown in Figure 11 with 22.5°, 45°, 90° and 180° phase bits[6]. Starting in the upper right with the 180° bit, the microwave signal travels counterclockwise through the 45° (upper left), 22.5° (lower left) and 90° (lower right)

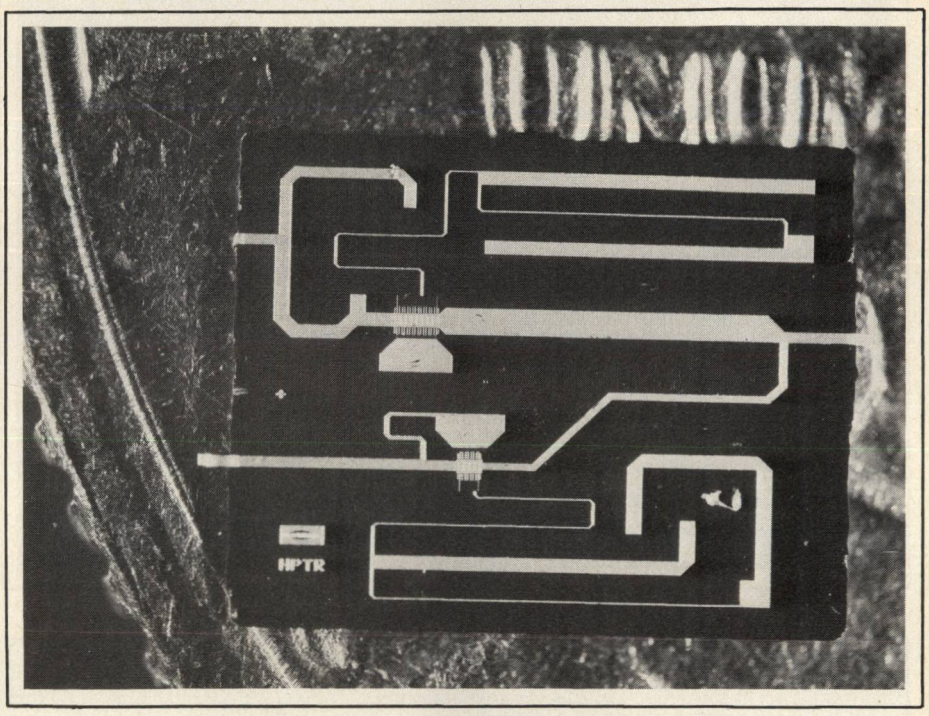

Fig. 10 Finished 10 W TR switch chip.

bits, exiting on the right edge of the chip. The circuit is passive and reciprocal so that the signal can equally well traverse this path in the opposite direction. The chip size is 6.4 x 7.9 x 0.1 mm.

The schematic circuit diagram of the four-bit phase shifter is shown in Figure 12. The 22.5 and 45 degree bits are designed to provide constant phase shifts over the frequency bandwidth using the loaded line technique. Each loading stub is composed of a suitably designed three section transforming and matching network which is terminated by a 1200 μm switch FET. The principle of operation of this circuit and of the ones using PIN diodes is the same.

The 90° and 180° bits are designed using the switched-line technique. Note, however, that instead of the conventional four switching elements, only three 800 μm switch FETs are used in these circuits. Equal insertion loss between two phase states is maintained by designing the short and long arms of the phase shifter at different impedance levels.

For all bits, the switching is performed only through the gate control voltages and no other bias is required for the operation of the phase shifter. Thus, rf microstrip lines do not carry any dc voltage (in fact, they are dc grounded) and therefore there is no need for dc blocking capacitors between individual phase bit circuits.

Experimental performance of the phase shifter indicates 5.1 $\pm$ 0.6 dB insertion loss with 16 distinct phase states between 0° and 360°[6]. The performance of the phse shifter is satisfactory for typical phase array applications. Their small size, negligible dc power requirements and subnanosecond switching times make the monolithic phase shifters good candidates for future frequency-agile airborne phased-array systems.

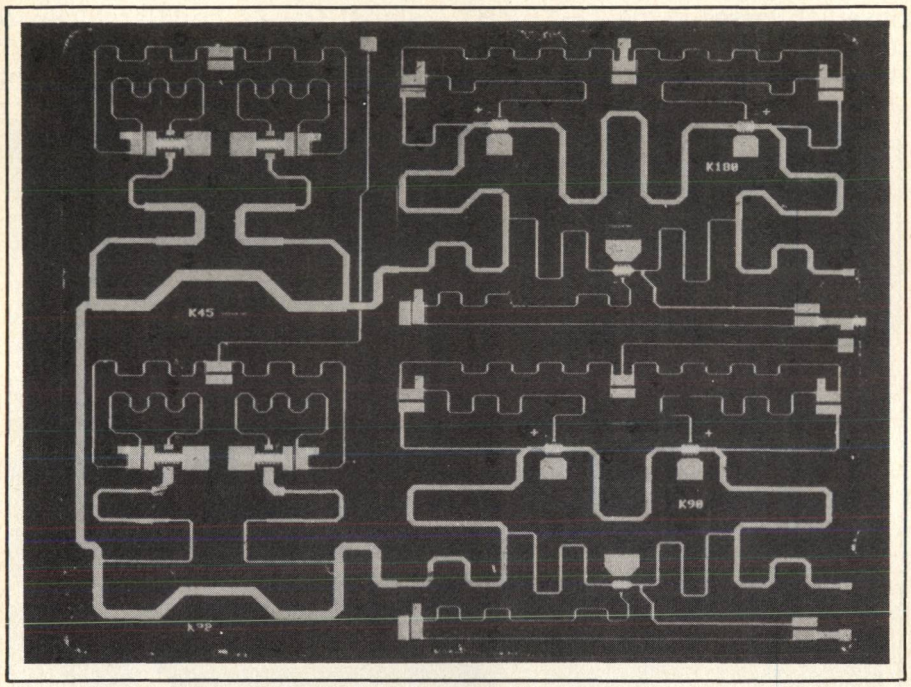

Fig. 11 Four-bit passive phase shifter chip.

Conclusions

The GaAs FET is examined in detail as a microwave frequency switching element. Its equivalent circuit as a switch is related to device geometry and channel

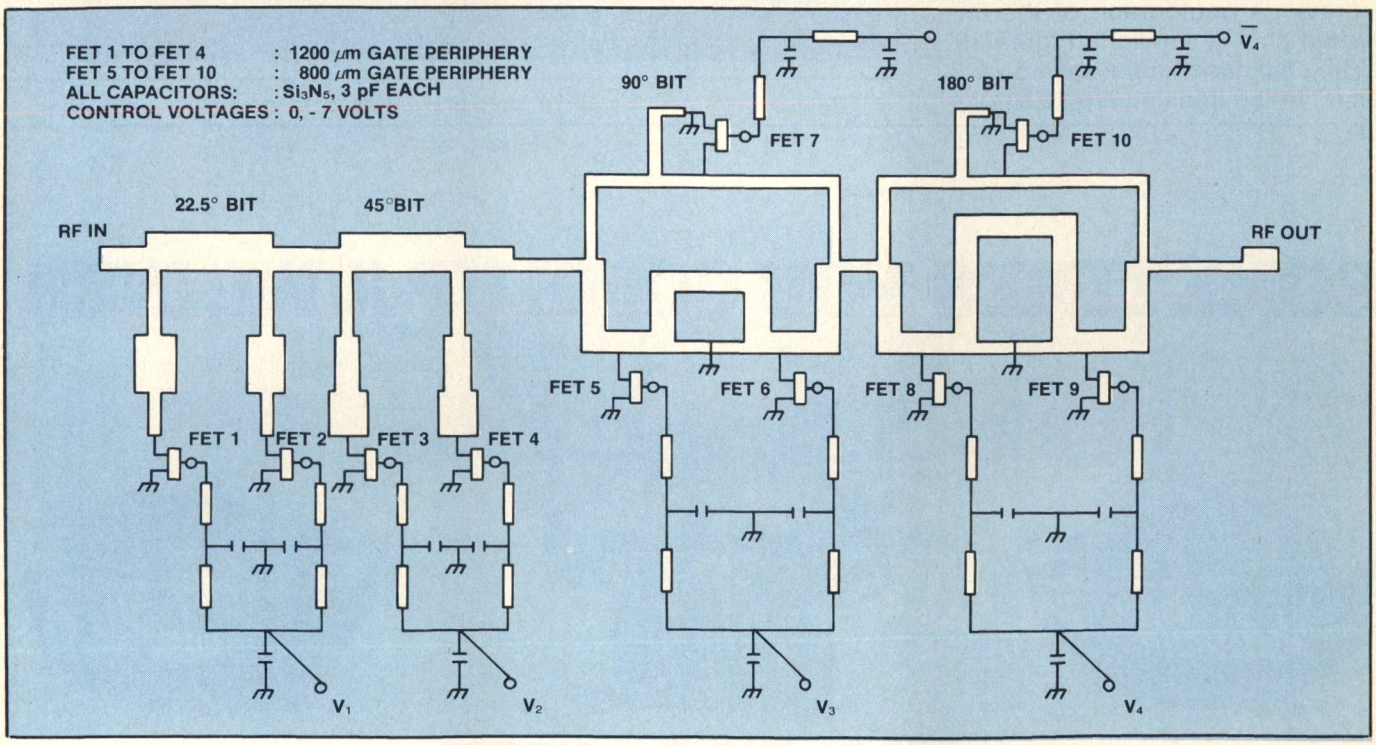

Fig. 12 The schematic circuit diagram of the four-bit phase shifter.

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parameters. The rf circuit design considerations characteristic of FET switching circuits are discussed with examples from recent monolithic circuit designs. These examples demonstrate the versatility of GaAs FETs as switches.

When circuit size, dc power consumption, switching speed and producibility in large quantities are of prime importance, GaAs monolithic FET switch circuits will lead the way for future systems applications.

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Yield Considerations in the Design and Fabrication of GaAs MMICs

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Introduction

Monolithic Microwave Integrated Circuits (MMICs) fabricated on GaAs substrates are revolutionizing microwave component and systems design.[1] The ultimate impact of this new technology on future microwave systems will be determined by the production yields that can be achieved for chips at a given level of performance. Not only will the attainable yields determine system cost/performance tradeoffs, but they will also delimit the extent to which MMIC chips will reach higher levels of system integration with commensurate reduction of size, weight and increased reliability.

At the present stage of development of GaAs MMIC circuitry, the emphasis is on achieving state-of-the-art performance comparable to or better than that of traditional MIC components. Application areas for MMICs will be highly sensitive to realization of equivalent or superior performance to MIC technology with additional advantages of reduced size, weight, and/or cost. Some applications will be more sensitive to size, weight and reliability considerations and others will be more sensitive to cost factors. MMIC yield will be the most significant factor in determining both chip cost and level of integration, and therefore, achievable yields will be a determining factor in the competitiveness of MMIC technology with established microwave circuit fabrication techniques.

The complexity of an individual MMIC chip can range from the component level to the subsystem level of circuitry as shown in Table 1. It may be seen from the table that the potential range of functionality of MMICs forms a hierarchy which spans from the individual circuit level to complex electronic subsystems on a chip. Realization of higher functionality MMICs will depend on achieving high overall yields which in turn depend on high component circuit yields.

TABLE I
MMIC CIRCUIT TYPES

I. Component Circuits:
- Broadband Amplifiers
- Low Noise Amplifiers
- Mixers (GaAs FET or Schottky Diode)
- Voltage Controlled Oscillators
- Power Amplifiers
- Binary Phase Shifters
- Microwave Switches

II. Functional Blocks:
- Integrated Receiver Front End
- Frequency Synthesizer (PLL)
- Multi-Bit Phase Shifters
- MSK Modulator/Demodulator

III. Multi-Functional Subsystem:
- T/R Module for Phased Array Radar
- Digital Radio Transmitter/Receiver
- Receiver/Signal Processor
- Television Receiver and Channel Selector for DBS

For a given degree of complexity it is possible to partition the circuitry so that MMICs of lower functionality may be interconnected using MIC technology to achieve the desired system performance. The unique advantages of MMIC technology such as small size, light weight, high reliability, and low cost, however, are all enhanced by achieving as high a degree of circuit integration as possible consistent with acceptable overall yields. Therefore, it is seen that the yield issue will be crucial in determining the eventual system impact of GaAs MMIC technology.

Production yields of high performance GaAs MMICs will be determined by the following salient factors:

- GaAs FET and Schottky Diode Yield
- Passive Component Yield
- Distribution of Element Values (Active and Passive)
- Circuit Performance Sensitivity to Element Values
- Chip Size

The above factors are dependent upon both design approach and fabrication technique. Approaches which are consistent with high production yield of GaAs MMICs are discussed, and representative examples of application of these considerations are described in the ensuing sections.

Design Considerations

A major design consideration for high yield (and associated lower

cost) is to minimize circuit size. For a constant percentage of good circuits, small size implies more circuits per wafer and therefore higher yield per wafer. However, to obtain a constant "good circuit" percentage on smaller chips, it is necessary to minimize the "critical circuit area" of each chip, i.e., the area sensitive to random failure modes due to contamination, mask defects, etc. Active devices and capacitors are most sensitive to these defects, while inductors, transmission lines, air bridges, and resistors are susceptible to a lesser extent. In addition, process related defects must be minimized by careful process design.

Engineering tradeoffs are necessary in the design of high yield circuits since the requirements for small size and use of a minimum number of "highest risk" elements are often contradictory. For example, broadband active matching consumes much less GaAs real estate then conventional passive reactive tuning elements. However, extra FETs are used which could adversely effect yield although RF performance may be enhanced by the use of active devices. Many similar cases exist, where either active or passive versions of a circuit could be designed. Usually the passive circuit is substantially larger but has higher yield. Examples include power dividers, phase shift networks, directional couplers, and many other components traditionally fabricated as passive circuits. The optimum compromise selected depends on actual processing yield for each of the various components, and no universal compromise exists. Continuous monitoring of yields is needed to make intelligent tradeoffs as the processing technology matures. However, as yields improve, the compromise tends to favor small chips and more active devices. An important additional advantage of this approach, and an indication that GaAs MMIC technology is maturing, is that chips of subsystem complexity can be seriously considered while maintaining reasonable chip size.

In addition to these general design guidelines, many specific circuit design and layout considerations can significantly increase yield. Some of these, such as capacitor and FET design rules, are dependent on the selected process and will be described later in this paper. Others are strictly circuit considerations which will improve the yield independent of processing techniques. Designs which minimize sensitivity to process variations will produce the highest RF yield. Feedback design is one of the most successful of these techniques at lower frequencies where the associated gain penalties are acceptable. At higher frequencies computer aided design techniques can be utilized to minimize circuit sensitivity to those elements most likely to vary, such as FET gate-to-source capacitance.

As in lower frequency silicon integrated circuits, resistance and capacitance ratios are more accurately controlled than the absolute magnitudes of these components. Designs based on ratios of similar element types will result in higher circuit yields. FET saturation current (I_{DSS}) will also be inversely proportional to resistor values provided the FET active layer is formed by the same ion implant used for resistor fabrication. This advantage, most useful in bias circuit design, is partially lost when high performance FETs with recessed gates are required in the circuit. The use of FETs as active loads or other bias control devices will retain bias tracking but could adversely affect noise and power performance in some designs.

Transmission line impedance variations also track across the chip (via a non-linear relationship) since they are formed with a common GaAs substrate thickness and metalization process. Although not often used in the design process this coupling simplifies sensitivity analysis, since only one common parameter (substrate thickness for microstrip lines) needs to be examined.

Fabrication Techniques

An ion implantation based process has been developed for the fabrication of Gallium Arsenide MMICs incorporating active devices, RF circuitry and all bypass capacitors. Multiple, localized ion implantation is used for forming optimized active layers and n^+ contacts for low noise and power FETs, mixer diodes, etc. Contact photolithography is used for all pattern steps. Plasma enhanced CVD silicon nitride is used as the dielectric in metal-insulator-metal (MIM) capacitors and as the insulator in a two level metalization process. Excellent uniformity and reproducibility of MIM capacitors, has allowed their use for both RF tuning and bypassing. Except for resistors, all microwave circuitry, air bridges, and beam leads are on the second metalization level which is electroplated to a thickness of 2-3 μm to minimize losses. Backside via holes are etched where necessary. An overview of the fabrication process is presented here and yield limiting factors which have been investigated are discussed.

Figure 1 is a schematic drawing of the various active and passive components comprising an MMIC. These include low noise and power MESFETs, Schottky barrier diodes, thin film and bulk resistors, MIM capacitors for RF tuning and bypassing, transmission lines, air bridges, and backside via holes. Fabrication of an MMIC begins with the synthesis of doping profiles for FET active layers, n^+ contacts and bulk resistors by localized Si^+ ion implantation in qualified semi-insulation GaAs substrates. Substrate qualification consists of sampling the front and the tail of the ingot under consideration and checking the doping profile for a standard implant-cap-anneal cycle. Activation, pinchoff voltage uniformity, and electron mobility are measured and compared with design specifications to determine the suitability of the ingot for MMIC fabrication. The isolation provided by unimplanted regions of the S.I. substrate after undergoing an annealing cycle is also checked. A sheet resistance $\geq 10^7\ \Omega/$ is required for passing this test. Data obtained on test wafers from different lots show that I_{DSS} uniformity over a $\sim$ 10 cm^2 wafer before gate recess is typically better than 5% (2 σ) and, for constant implantation dose,

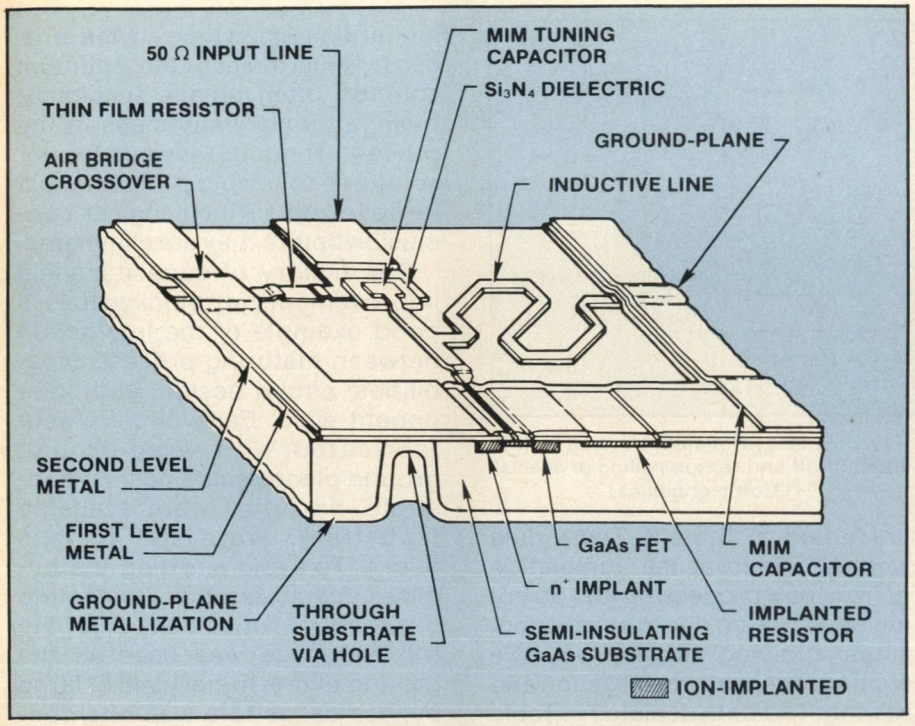

Fig. 1 Schematic drawing of typical MMIC.

reproducibility from run to run is approximately 10% (2σ). These data were obtained using both Bridgman and LEC (undoped and Cr doped) substrates. I_{DDS} reproducibility can be improved by a slight dose adjustment for each ingot as determined by the qualification data.[2]

Following active layer formation, ohmic contacts are formed by sequential evaporation of Au-Ge and Ni, liftoff, and alloying at 450°C. This contact formation technique results in reproducible low resistance contacts. Typically, $r_c \simeq 1 \times 10^{-6}\ \Omega\,cm^2$, and this value is maintained through the entire MMIC fabrication process which includes two 250°C silicon nitride deposition steps.

After contact metalization, the submicron gates are defined by contact photolithography and liftoff. Gate yield can be a significant circuit yield limiting factor. In addition to broken gates, other defects such as those induced by excessive wafer handling, poor source-drain metal definition, and short circuits caused by metalization defects associated with contact lithography are presently limiting gate dc yield. Short circuits caused by misalignment (due to mask runout, wafer warpage, mask-wafer bowing, aligner limitations, etc.) become important when gate source gaps are reduced to improve device performance. In order to maximize gate yield several precautions are taken. These include monitoring wafer flatness and ensuring that it is in the range of $\pm$ 1 μm/inch after capping and annealing, and using 0.090 inch thick masks for minimum distortion during contact printing. Typical dc yield of a 500 μm wide FET with a 4.8 μm source-drain gap is 92%.[2]

Ti/Au first level metalization provides overlays for ohmic contacts and the lower electrodes of MIM capacitors. This pattern is formed by dielectric aided liftoff to achieve the rounded edges necessary for good capacitor yields. Ion milling and some other liftoff techniques[3] have also been used successfully for this metalization step. A 6000 A layer of silicon nitride is deposited over the first level metal using plasma enhanced chemical vapor deposition (PSN). This forms the dielectric for MIM capacitors and the insulator for second level metal crossovers. Finally, the second metal layer is defined by photolithography and gold electroplating to a thickness of 2-3 μm. The second level metal provides the top electrode of MIM capacitors, plus interconnects, air bridges and other microwave circuitry.

The uniformity, reproducibility, and dc yield of MIM capacitors has been studied. Data on the first two aspects indicate good control of the thickness and dielectric constant of PSN. A run to run variation of $< 8\%$ (2σ) has been achieved over a period of ~ 2 years. Variation over a wafer is considerably less. Such control has made possible the use of MIM capacitors for RF tuning as well as bypassing applications.

DC yield of MIM capacitors depends on both the area and the length of overlap periphery (Figure 2) between the first and the second metalization levels. It has been possible[2] to obtain a good fit of measured dc yield data to an equation of the form:

$$Y = 1 - \alpha A - \beta P$$

where,

Y = DC yield of MIM capacitor
A = Capacitor area
P = Overlap periphery between first and second metalization levels using linear regression techniques. The area dependence of capacitor yield is due to pinholes in the nitride. In practice, pinholes

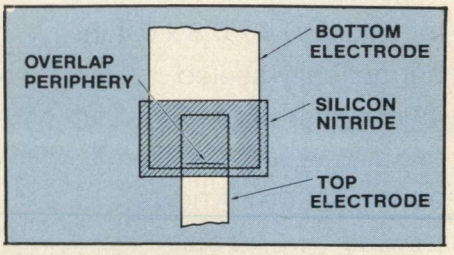

Fig. 2 Typical MIM capacitor with overlap periphery defined.

are associated with debris on the wafer, metal splattering during first level metalization etc., and can be reduced by controlling these factors. The periphery dependence arises due to sharp edges (obtained by direct liftoff, Figure 3a) which are not well covered by PSN and usually result in a short. Rounded edges, as obtained by ion milling or special liftoff techniques[3] (Figure 3b), are more reliably covered by PSN and cause fewer shorts.

Preliminary data on dc probe plus visual (microscopic) circuit yield of three different circuits is

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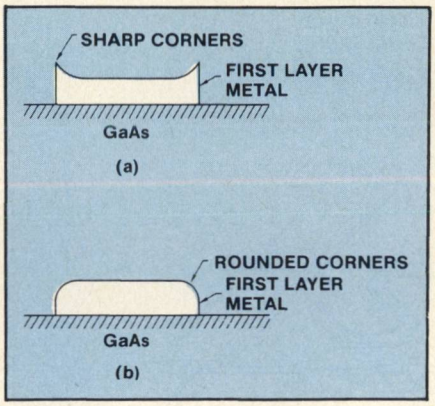

Fig. 3 First layer metal definition by (a) direct liftoff and (b) ion milling or special liftoff techniques.

presented in Table 2. These data were obtained at the completion of front end processing and do not include attrition due to subsequent steps involving thinning, via hole etching, backside metalization and sawing. The data depicted in Table 2 are commensurate with individual component yields and indicate the potential for achieving high overall yields of functional MMIC modules with subsystem complexity.

TABLE II
DC CIRCUIT YIELD

	Buffer Amplifier	Driver Amplifier	Power Amplifier
Total Gate Periphery (mm)	0.2	1.0	1.98
Source-Drain Gap (μm)	3.8	4.8	4.8
Total MIM Capacitance (pF)	20	49.4	50.8
FET Yield (%)	81	86	59
Capacitor Yield (%)	97	88	76
Circuit Yield (%)	78	76	47

Data on component yield are obtained in the process of correcting known yield problems. The "weakest link" technique, i.e., detecting the most serious problem, developing process and/or circuit changes to increase yield, and then determining the new yield limiting factors, is a powerful method of increasing circuit yield. Proper application requires sufficient processing volume to obtain meaningful yield data, and detailed consideration of the entire processing sequence after every proposed change in fabrication. It is common to solve one yield problem by inserting more severe limitations elsewhere in the process. Nevertheless, the optimum solution often entails simultaneously altering many steps in the process. Therefore seemingly poor solutions to a yield problem must be followed to their logical conclusion before they are eliminated.

The history of capacitor yield improvements at Rockwell is a good example of the interaction between maturing process capabilities, circuit design, and component yield. Early circuits were fabricated with wrap-around ground planes since no thru-substrate via holes were available (substrates were still 10 mils thick). To avoid shorting the bypass capacitors while connecting the sheet ground to the chip, the top electrode was used as the ground plane. Initial yield of large bypass capacitors was often below 10%, and they were quickly identified as the "weakest-link."

As described previously, the major yield problems were pinholes in the dielectric (silicon nitride) and "spikes" on the edges of the bottom layer metal. Steps were taken to round the metal edges and reduce contaminiation, resulting in significant yield improvements. As the process matured via holes were added and wrap-around grounds could be eliminated. Placing the ground on the bottom layer allowed the edge (with potential spikes) to be outside the top metal around most of the capacitor periphery. Yield was once again improved at the same time RF performance was improved by lower grounds. Finally, the addition of the high yield air bridges (needed for low capacitance crossovers) allowed the to-

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tal elimination of overlap induced shorts. Yield of large bypass capacitors is now over 90% and they no longer represent the weakest processing link.

Based on these and other similar yield considerations, many circuits have been successfully designed and fabricated. Three representative examples will be summarized here. The first[4] is a broadband amplifier initially designed over two years ago for the Army which still dramatically demonstrates the power of active matching techniques. High FET yield allows the use of two extra active devices to reduce chip size and improve performance without

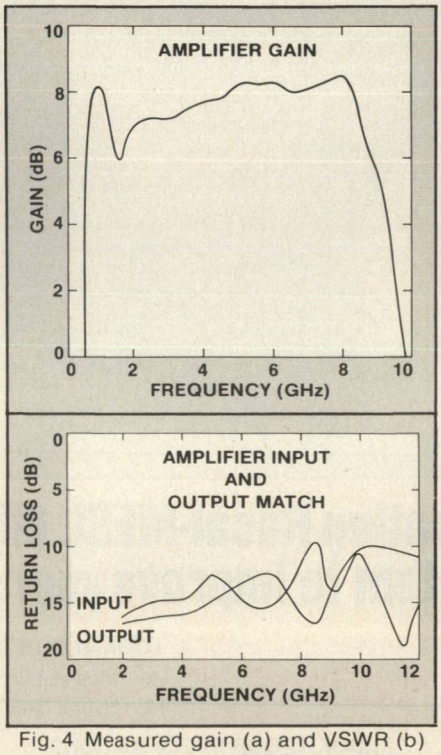

Fig. 4 Measured gain (a) and VSWR (b) of the broadband MMIC amplifier.

significant yield penalties. Figures 4a and 4b show the measured gain and VSWR performance respectively. Initial yield was poor due to capacitor shorts (the chip has over 130 pF total capacitance) but was later improved. This device prompted much of the capacitor yield studies which lead to the present capacitor design.

The second circuit example is a two stage 8 GHz amplifier developed for the Navy[5] which demonstrates the need for extensive computer modeling. Accurate element and parasitic models allowed layout on a two millimeter square chip with all passive matching circuits. On chip resistive bias networks and bypass capacitors reduced external connections to just two RF and two dc lines (plus a

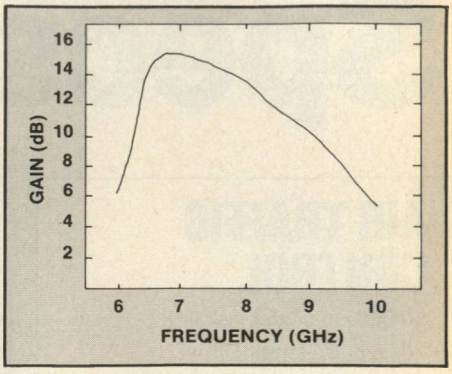

Fig. 5 Measured gain of a two stage monolithic amplifier.

sheet ground). Figure 5 shows the measured gain of this amplifier chip.

The final example[6] demonstrates the advantage of feedback which reduces sensitivity to process variations. At low frequencies resistive negative feedback provides broadband input and output match with flat gain and toler-

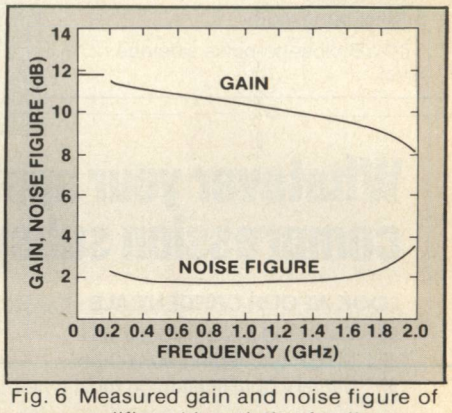

Fig. 6 Measured gain and noise figure of an amplifier with resistive feedback.

ance to variations in the active and passive device parameters. Figure 6 shows the measured gain and noise performance of this type of amplifier. Since a large device is needed to obtain sufficient transconductance to operate in the resistive feedback mode, output power in excess of 20 dBm is obtained as a byproduct of this design method.

All three amplifiers described above can be fabricated with high dc yield. RF yield will vary between them, with the feedback amplifier least sensitive to process variations and the broadband

amplifier most sensitive. It should be noted that active matching and feedback techniques are particularly insensitive to process variations, and both will be more widely used in the future.

Conclusions

The above descriptions of design approaches and fabrication techniques to achieve high yield of GaAS MMICs set the stage for consideration of the impact of yield on chip cost and multicircuit capability. To first order, the yield of higher complexity MMICs can be approximated as the product of the yields of the constituent circuits. Referring to the hierarchy of MMIC circuit types described earlier, it is seen that chip complexity in terms of the number of component circuits on chip naturally falls into one of the following ranges:

MMIC FUNCTIONALITY AND CHIP COMPLEXITY

FUNCTIONALITY	CHIP COMPLEXITY (# OF CIRCUITS)
Single Component	1 to 3
Functional Block	4 to 10
Multi-functional Subsystems	11 or more

where, in the above classification scheme, each gain stage of an amplifier is counted as a separate circuit for the purpose of determining complexity.

From the preceding sections it may be seen that the yield for a single (medium power) amplifier stage may range between 50 and 80% including dc testing and microscopic visual inspection. Microwave testing may be expected to incur an additional yield factor which may range from 50 to 90% depending on design sensitivity and process control. In the simplest analysis, then, the yield of a single component MMIC could be as high as 37 to 72%, assuming the best dc yields observed, and an RF yield of 90%. On the other hand, the best yields for functional block MMICs based on the same assumptions are in the range of 3.7% to 27% and the best yields for multifunctional subsystem MMICs are in the range of 0 to 2.7%. Obviously the present analysis is over simplified since the multi circuit yields quoted above are estimated by taking the nth power of the estimated individual circuit yield. However, just from doing the above exercise it becomes obvious that multicircuit MMIC yields may be quite low even with respectable single stage yields.

The point of all this talk about yields is to suggest that in the hierarchy of MMIC functionality described above, a point is reached at which it no longer makes sense to put additional circuits on a single chip, and that, for reasons of cost and overall yield, the circuitry should be partioned and interconnected using MMIC technology to realize the total functionality. The level of complexity at which the partitioning should occur is dependent on both the attainable yields at a given stage of development of the technology and on the cost sensitivity of the application as well as competition for the same application from existing technology. At the present time, it appears feasible to develop and use MMIC technology at the component level (up to several stages) and to a certain extent at the functional block level albeit with somewhat lower yields. As the GaAs MMIC technology matures, it is anticipated that multifuntional subsystem chips will become technically and economically feasible, and that functional block type chips will become highly competitive with other microwave circuit approaches for applications with a substantial volume requirement.

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D. R. Decker, *manager, Microwave Devices, received his B.S., Physics from North Carolina State University; M.S., Physics and Ph.D., Electrical Engineering from Lehigh University. Since joining the Rockwell International Microelectonics Research and Development Center in 1978, Dr. Decker had been active in the research and development of GaAs microwave devices. His current interests are in the design and development of GaAs monolithic microwave integrated circuits for broadband amplifiers, power amplifiers, balanced mixers, digital phase shifters, feedback amplifiers and integrated receiver front end applications, development of very low noise GaAs FETs, and modeling and design techniques for large-signal microwave ciruitry.*

Prior to joining Rockwell, Dr. Decker has had extensive experience in microwave device and circuit technology. In 1976, he joined the National Radio Astronomy Observatory in Charlottesville, Virginia, where he was engaged in research and design of low noise millimeter wave receivers. In 1975, he joined Hewlett Packard Co. in Palo Alto, California, where he worked on low noise and high power GaAs FETs and circuits. Dr. Decker has two patents in GaAs FET Technology. and is a senior member of the IEEE. ■

Broadband Monolithic Integrated Power Amplifiers in Gallium Arsenide

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Introduction

The use of monolithic microwave integrated circuits is necessary to maximize performance and reduce cost of power amplifiers (1-10 watts) at S- to X-band frequencies and above. Performance is enhanced because the close spacing of field effect transistors (FET's) used in the multistage amplifiers allows almost identical device characteristics and, in addition, the tuning elements in microstrip and lumped element forms can be fabricated close to the active elements, thereby reducing losses. Cost is reduced because silicon-like processing can be used on wafers ground to 2 in. diameter with orientation flats resulting in DC yields of up to approximately 40% for 2-stage, 1 watt amplifiers (50 amplifiers/wafer). Low costs are necessary for phased array applications where many thousands of identical amplifiers are employed. The hybrid realization of similar amplifiers is considerably more expensive.

This paper describes the development of two designs of 2-stage monolithic integrated amplifiers in gallium arsenide covering the 5 to 10 GHz and 8 to 12 GHz bands. The amplifiers were fabricated using ion implantation of Si^{29} directly and selectively into undoped, semi-insulating gallium arsenide grown by the Czochralski technique in-house at Westinghouse.

The passive elements in the amplifiers are a combination of microstrip and lumped elements to produce low-loss impedance-transformers, power splitters and power combiners. Both interdigital and overlay Metal-Insulator-Metal (MIM) capacitors have been used in the circuits. The MIM capacitor is favored because of its smaller size and higher Q. Together with the submicron gates of high frequency amplifiers, the MIM capacitor is the lowest yield element in these monolithic circuits (~95%). Both via construction (connections between the ground plane on the back of the wafer and grounded elements on the front of the wafer) and air bridge fabrication have yields that are better than 99%.

RF Design Methods

The cost and performance advantages of minimizing chip size preclude the commonly used balanced amplifier approach to wideband performance since it requires

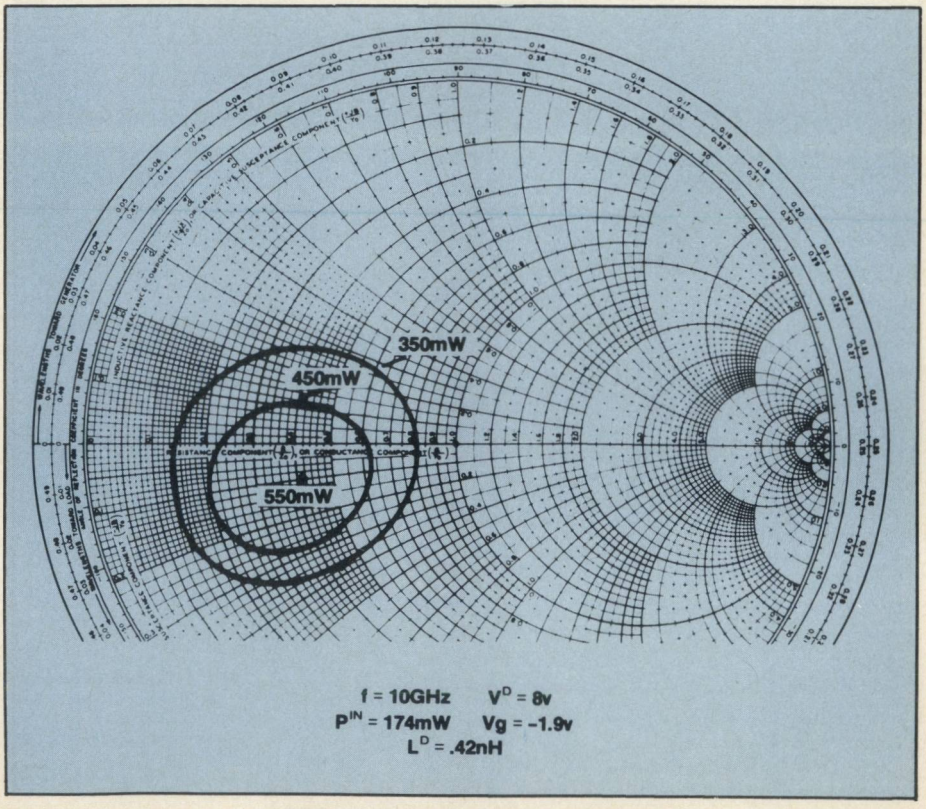

Fig. 1 Load pull circles for 1200μ FET.

relatively large quadrature couplers on the input and output of each stage in addition to matched amplifier pairs. At Westinghouse a single ended approach was taken, which is based on load-pull characterization of the FET's and has been used to design a number of 2-stage, 5 to 10 GHz and 8 to 12 GHz monolithic amplifiers with power outputs of 1 watt. The approach may be summarized as follows:

- For a given fixed input power level, load-pull contours are plotted corresponding to constant power output at each frequency.
- The output circuit (or interstage circuit in the case of the first stage) is designed to present an impedance locus which crosses these constant power contours in a manner to provide constant power at each frequency.

Thus, the output circuit provides the optimum load impedance at the highest frequency of interest while selectively "de-optimizing" the load impedance at lower frequencies to provide constant power (and gain).

The "load-pull" measurements give data on how the output power of each FET varies as a function of the load impedance presented to it. The load impedance is varied electronically to any value[1] and the corresponding output power measured, resulting in a series of constant power contours for a fixed input power and bias point generated at each frequency of interest in the design band. Such a set of contours is shown in Figure 1 for a 1200 μm first stage FET at an input power of 174 mW at 10 GHz. The bias point for this FET is V_{DS} = 8V, V_{GS} = -1.9V, and I_D = 150 mA. At each frequency there is only one load impedance, which when presented to the FET, results in maximum output power for a given input power. At 10 GHz, the 1200 μm FET has a maximum power output of 550 mW. This power level is particularly important since, according to our design approach to gain equalization, the maximum output power at the highest frequency in the design band governs the output power of that stage across the band.

At 7 GHz (Figure 2), the maximum output power has risen to 695 mW. The 550 mW level, which was attainable by only one load impedance at 10 GHz, is now attainable by impedances lying on the locus shown at 7 GHz since the FET must be power mismatched to produce less than maximum output power. The loci of impedances at 5 GHz producing the 550 mW level is even larger since the mismatch must be even greater.

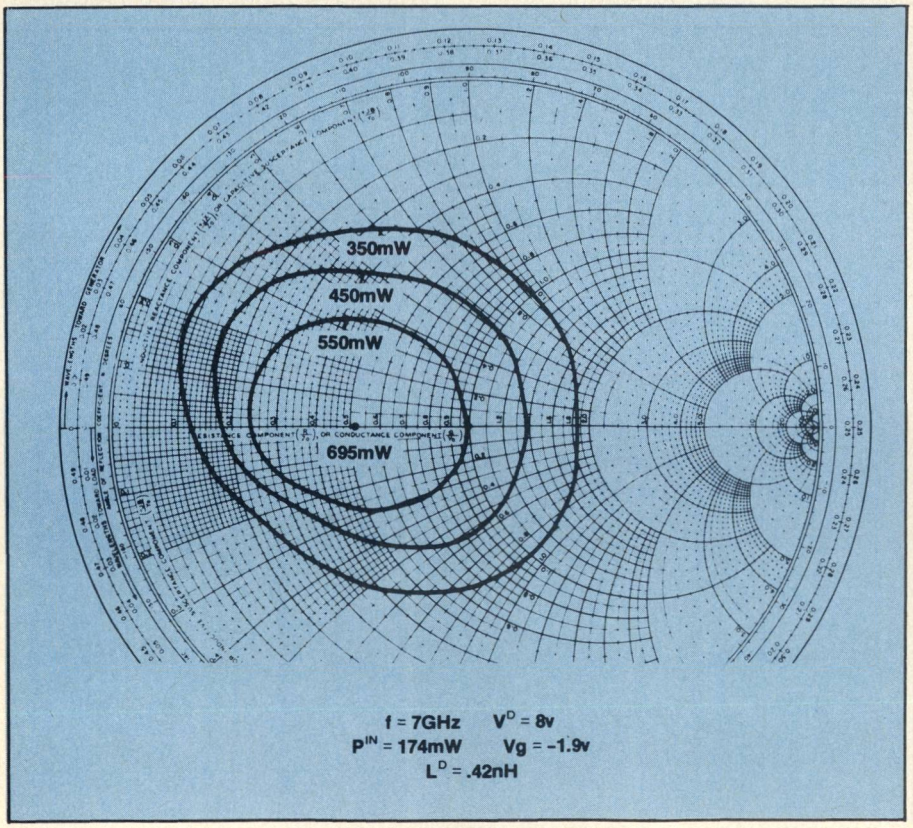

Fig. 2 Load pull circles 1200μ FET.

If the 550 mW load-pull circles at each frequency are all plotted on one Smith chart, the composite contours shown in Figure 3 result. Note that the composite contours are shifted more to the inductive end of the Smith chart than the individual frequency contours. This is due to the fact that the bondwires used to connect the FET to the test fixture have been accounted for since they obviously are not present in the monolithic amplifier. The composite contours represent not only constant output power, but also constant gain.

With these composite load-pull contours determined, the design problem becomes one of designing the output circuit (or interstage circuit in the case of the first stage) to present an impedance locus which crosses the constant power contours in a manner to provide constant power at each frequency. Such a procedure is complicated and has been described in detail in an earlier article.[2]

Once the initial lumped element circuit parameters and basic circuit topology have been determined, the circuit is converted to a distributed model. To do this, the lumped inductors are replaced by short pieces of microstip transmission line. Shunt parasitic capacitances associated with interdigital capacitors over a ground plane are also added and the entire network is optimized using a special computer algorithm to optimize the impedance locus fit to the composite load-pull contours.

This design procedure has been used to realize a 5 - 10 GHz monolithic amplifier and an 8 - 12 GHz monolithic amplifier incorporating a 1200 μm periphery power FET and a 2400 μm periphery power

FET. The design goals were 1 watt of output power and 10 dB gain for the 5 - 10 GHz chip and 0.6W output power for the 8 - 12 GHz chip.

IC Fabrication Techniques

— Material Growth

The gallium arsenide semi-insulating substrates used for the fabrication of monolithic integrated circuits are produced in-house from <100>-oriented, single crystals grown by the liquid encapsulated Czochralski (LEC) technique using a Melbourn high-pressure puller (Metals Res. Ltd.). The crystals are pulled from the melt contained in a pyrolytic boron nitride (PBN) crucible following compounding in-situ; a liquid B_2O_3 encapsulant and inert gas overpressure are employed to prevent As sublimation which would result in low resistance, nonstoichiometric crystals.

Careful elimination of electrically active impurities, particularly Si which can be introduced by SiO_2 crucibles, eliminates the need to counter-dope with Cr to compensate residual shallow donors. These crystals exhibit state-of-the-art chemical purity and minimize residual impurity activation during processing. As grown, the material exhibits sheet resistivities (R_s) of 3×10^8 Ω/square and mobilities of 5000 cm^2/volt-sec. This mobility can be attributed to $\sim 1\times10^{16}/cm^3$ residual shallow acceptors (carbon) and an equivalent density of ionized deep donors (EL2).[3] The concentration of the residual shallow acceptors varies from $1\times10^{16}/cm^3$ at the seed end of the crystal to $2\times10^{16}/cm^3$ at the tang end and this variation ($1\times10^{16}/cm^3$) represents the change in activation of the Si^{29} implant that can be expected along the crystal.

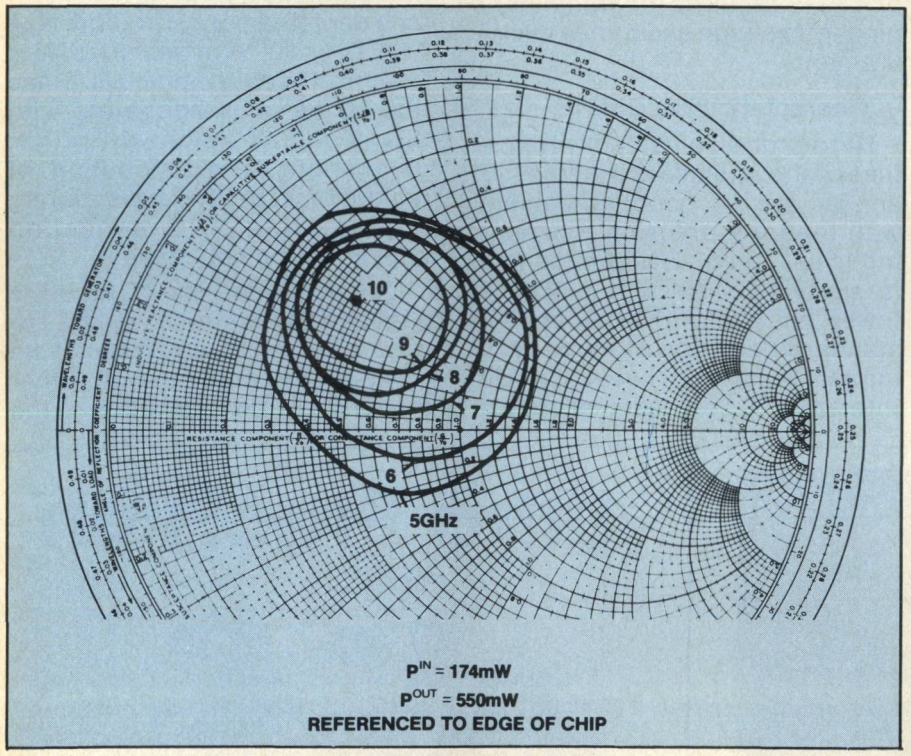

Fig. 3 Composite load pull circles 1200μ FET.

The implantation process in use preserves $R_s \geq 2\times10^7$ Ω/square and $\mu_H > 4000$ cm^2/volt-sec in unimplanted areas. The crystals are ground to 2″ diameter and flatted along <100> directions prior to on axis slicing. Lapping and polishing yields approximately 100, 0.020″ thick wafers.

— Ion Implantation

Implantation processing originates with plasma deposition of a 900 Å Si_3N_4 primary encapsulation layer on the front surface. This layer remains on the surface through processing to prevent mechanical damage and/or chemical contamination as well as to

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prevent dissociation during the implant anneal. The nitride is deposited at 340°C and 70 Å/min using a plasma-enhanced reaction to minimize substrate decomposition and interface stress. 2500 Å of phosphosilicate glass (PSG) deposited after the Si_3N_4 serves as both an implantation mask and a registration layer; the PSG layer remains on the wafer through the implant anneal and is plastic at the annealing temperature, thereby reducing stress.

Contact photolithography and ion milling is used to open windows to the PSG/Si_3N_4 interface for ion implantation. Implants are made at two different Si^{29} ion energies through the 900 Å thick Si_3N_4 at ambient temperature to provide an approximately flat chemical profile. The depth at which the peak concentration falls to half (λ_0) is 2750 Å in the optimum design of material for 8 - 12 GHz FETs. This requires energies of 260 KeV and 125 KeV at dose ratios of 3:1.

After the stripping of the photoresist and the deposition of a second PSG layer the wafers are annealed through controlled cycles to 860° C for 15 minutes to activate the implant. Mechanical support of the wafers is required during this annealing step since the wafers become plastic and may deform at these temperatures.

Alignment marks are ion milled into the gallium arsenide surface using a combination of new photoresist mask and the existing PSG layer.[4] In this way precise alignment with the implanted areas is maintained. Test areas included in all mask sets permit deposition of Al C-V patterns for preliminary pinchoff voltage and profile measurements.

— Characterization Data

Net donor, electrical activity profiles of the implanted wafers after anneal are in good agreement with theory if diffusion broadening is assumed. This broadening is significant since it places a lower limit of $\approx$ 700 Å on the standard deviation of the Si doping profile at the channel-substrate interface. Deep level acceptor doping such as chromium improves interface abruptness at the expense of reduced channel activation and decreased depth reproducibility.

Analysis of Hall mobility data as a function of implant dose (D) yields the following equation for N_{SM}, the concentration of mobile charge in the FET channel:

$$N_{SM} + N_{sd} = \eta D - \lambda_0 N_A$$

where N_A is the density of residual acceptor like levels that must be filled to achieve a conduction n channel, η is the net donor activation efficiency, and N_{sd} is the surface depleted concentration. $N_A = 1.0 \pm 0.4 \times 10^{16}/cm^3$ and $\eta = 0.76 \pm 0.04$ in all qualified crystals. Since this N_A value is consistent with that found in as-grown wafers, generation or redistribution of residual acceptor levels during implantation and annealing appears to be negligible.

Detailed analysis of mobility data shows that the η value is the result of amphoteric doping of the GaAs by the implanted Si rather than incomplete activation of the

Si centers. All of the implanted Si appears as singly ionized, isolated donors or acceptors. It is also found that the Si amphoteric doping ratio is proportional to the square of the electron density at the annealing temperature which results in sublinear activation of the implanted Si for net doping densities greater than $2.5\times10^{17}/cm^3$. Mobilities of 5600, 4800, and 4400 cm^2/volt-sec are achieved for channel concentrations of 2×10^{16}, 1×10^{17} and $2\times10^{17}/cm^3$ respectively. Profile uniformity better than ±5% is achieved while the uniformity of N_{SM} as measured by Hall effect is better than ±2%. The full channel current uniformly in the FETs is ±4% across 2″ wafers. Pinchoff voltage uniformity measurements have shown $V_p = 7.1\pm0.1$ volts for $n = 1.5\times10^{17}$, $\lambda_0 = 2750$ Å implanted layers.

Metalization Technology

Following the implantation and activation of the Si^{29} implant ohmic contacts for the sources and drains of the FETs are deposited by a liftoff process on to the gallium arsenide using the alignment marks ion milled into the surface during the ion implantation processing. The metal used for the ohmic contacts consists of 1100 Å gold 12% germanium alloy, 500 Å nickel and 400 Å of platinum. This metal system is alloyed at 490° C for 10 secs in an argon-10% hydrogen atmosphere and the contacts thus formed are very reproducible from run to run and across the 2″ wafers with values of contact resistance less than 3×10^{-6} Ω cm^2, monitored routinely using the TLM method.[5]

The gates of the FETs are formed using contact lithography and masks made by E-beam[6] on 4-inch, 90 mil thick quartz plates. Two photoresist systems have been employed. The first of these is AZ1350J photoresist in combination with near-UV (405 nM) radiation and has resulted in gates down to 0.7 μm long. A chlorobenzene soak of the AZ1350J photoresist provides an overhang which greatly assists the liftoff of the gate metallization which consists of 500 Å titanium, 400 Å platinum and 6500 Å of gold. Dimensions down to 0.5 μm have been achieved using a double layer structure of a co-polymer of polymethyl methacrylate (PMMA) and 25% methacrylic acid (MAA) on top of a layer of PMMA and exposed by deep UV (210 nM) radiation.

Prior to deposition of the gate metals the gate region is wet chemically etched to a depth of 1000 Å to provide a recessed gate structure.[7] The etchant for the AZ1350J resist is a basic etch consisting of a 6% by volume of 30% hydrogen peroxide in a 2% solution of ammonium hydroxide. Since PMMA tends to be attacked by basic solutions the etch used for the double layer resist system employs a 2% HCl solution to replace the ammonium hydroxide.

Following testing of the now gated transistors, the circuit metallization is defined using a thick layer of AZ1350J (3.7 μm). The pattern places inductors on the surface of the gallium arsenide in the form of microstrip lines

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which are plated up to a thickness of 5 μm later in the fabrication process when the air bridges are formed. In addition, the interdigital capacitors or, in later designs, the bottom plates of metal-insulator-metal (MIM) capacitors are defined together with the drain interconnections on the FETs.

The circuit metalization is 11500 Å of metal which is composed of chromium (500 Å), palladium (1000 Å) and gold (10000 Å). For the M-I-M capacitor circuit designs an additional layer of chromium (500 Å) is added to provide good adhesion of the insulating layer (sputtered silicon dioxide). The dielectric for the M-I-M capacitors is bias-sputtered SiO_2, 3000 Å thick, that is patterned by lift-off using 2.5 μm of AZ1350J photoresist.

Interconnections of the sources of the FETs and the top plates of the MIM capacitors are formed by "air bridges" as shown in the scanning electron micrograph of Figure 4. The process consists of depositing a lower layer of AZ1375 photoresist (4 μm thick), which is then opened to expose the areas to be connected by the bridge. 500 Å of titanium and 500 Å of gold are then evaporated over the whole wafer and a second layer of AZ1375 (4 μm) is then used to define the bridge itself. The opened areas are plated up with gold to a thickness of 5 μm, the top photoresist removed and the thin gold and titanium layers chemically etched away. Removal of the lower resist layer completes the process and results in high yield (> 99%) rugged interconnections.

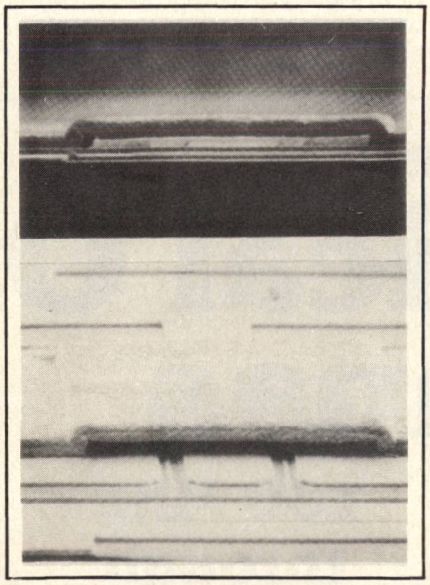

Fig. 4 Air bridge interconnection on GaAs monolithic circuit 5 μm high, 6 μm thick, 100 μm long.

The front of the wafer is now complete and the remaining steps are thinning of the slice, formation of vias and metalization of the back of the wafer. The slice is thined from 500 μm down to 100 μm to provide the correct spacing between the microstrip lines on the front of the wafer and the ground plane on the back. Thinning is accomplished by a combination of lapping in a semi-automatic jig and a final chem-mechanical polishing. A rough surface finish of the back of the wafer has been shown to have a deleterious effect on circuit losses.[8]

Air bridges and via holes are used, respectively, to interconnect the FET source pads and to provide low inductance source grounds. The via holes also improve circuit layout flexibility by permitting grounding of circuit elements interior to the chip. The positions of the vias can be clearly seen by their effect on the planarity of the first circuit metalization. Six vias are visible, four at the ends of the two FETs and two on the left hand contacts of a pair of capacitors in the interstage matching circuit at the center of the chip. A seventh via lies beneath the pad at the center of the output FET but is hidden by the thick (5 μm) metal plating on that part of the circuit. RF bypassing is accomplished using the off-chip capacitors located adjacent to the GaAs amplifier.

Vias are formed by wet chemical etching using a slighly preferential etch to produce cone-shaped holes through the 100 μm substrate. The AZ1375 photoresist pattern for etching is positioned using infrared alignment to the source pads on the front of the wafer. The vias and the back of the wafer are then coated by sputtering 500 Å of chromium and 10000 Å of gold followed by evaporation of additional layers of metal including nickel which acts as a barrier to the gold-tin alloy used to bond the finished chips to the

microwave test package.

The slice is then sawn into chips and those chips which have acceptable DC FET and passive characteristics are mounted and bonded into RF packages for testing.

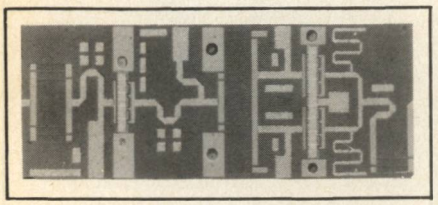

Fig. 5 5 to 10 GHz amplifier with interdigital capacitors.

Amplifier Performance

The design and fabrication procedures described above have been employed to produce 5 to 10 GHz and 8 to 12 GHz two stage amplifiers. Figure 5 shows a 5 to 10 GHz amplifier designed to deliver 30 dBm (1 watt) of output power with 10 dB gain on a chip 2 mm × 5.25 mm × 0.1 mm thick. The first and second stage FETs have total widths of 1200 μm (four 300 μm cells) and 2400 μm respectively. The gate lengths are 1 μm and each gate finger width is 150 μm. The matching circuits incorporate interdigital capacitors (5 μm fingers and 5 μm gaps) and inductors formed by short lengths of high impedance microstrip transmission lines. The capacitors occupy large areas of the chip at the input, center and output of the amplifier.

The output power as a function of frequency for this amplifier is plotted in Figure 6. It can be seen that, with 21 dBm input power (125 MW), the output power is 29 dBm (790 W out) from 5.3 to 9 GHz and approaches 30 dBm over parts of the band.

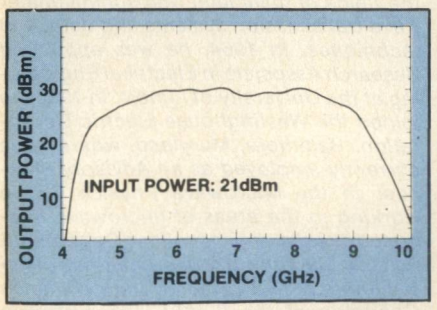

Fig. 6 Output power as a function of frequency for a 5 to 10 GHz amplifier with interdigital capacitors.

A considerable improvement in performance is obtained with later designs of amplifiers using MIM overlay capacitors in place of the interdigital capacitors. These capacitors provide a significant reduction in circuit size as well as permitting the placement of the RF bypass capacitors (5 to 20 pF) on the amplifier substrate itself. Six bypass capacitors can be seen in Figure 7 at the edge of an 8 - 12 GHz chip. The tuning capacitors at the center of the chip are now much smaller than their interdigital counterparts in the circuit shown in Figure 5. The amplifier shown in Figure 7 has gate lengths of 0.75 μm and is designed for the 8 to 10 GHz range to deliver 28 dBm (0.6 watts).

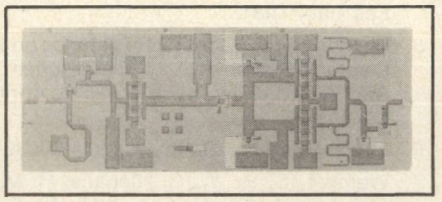

Fig. 7 8 to 12 GHz amplifier with MIM capacitors.

The measured output power shown in Figure 8 exceeds 30 dBm (1 watt) from 6.5 GHz to 11.6 GHz with 9 dB of gain. Improvements in the interstage circuitry are expected to improve the performance still further in the 8 to 10 GHz range.

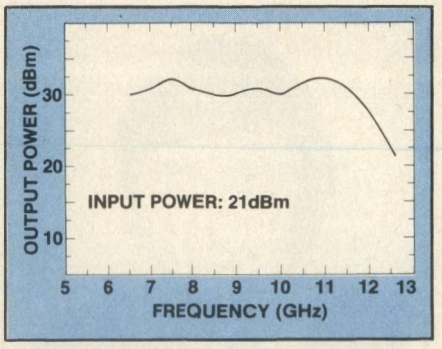

Fig. 8 Output power as a function of frequency for an 8 to 12 GHz amplifier with MIM capacitors.

Conclusions

The design methods, fabrication technology and gain-frequency performance of two wide band monolithic power amplifiers in gallium arsenide have been described. These devices show excellent performance at the 1 watt level and are expected to play an important part in the realization of phased array systems in the future.

[Continued on page 94]

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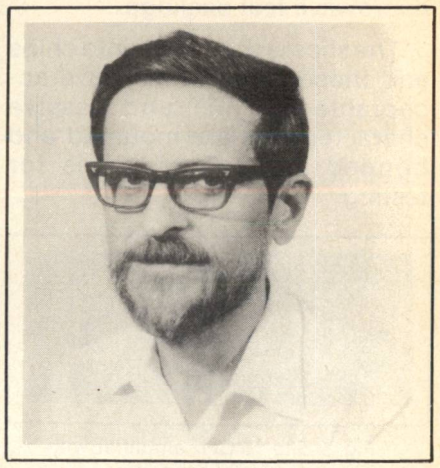

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Hybrid vs. Monolithic Is More Monolithic Better?

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Over the past two years a glut of papers, panel sessions, and workshops have described the benefits and shortcomings of monolithic IC's. The proponents of monolithic circuits have shown how they will be used in phased array radar and direct broadcast television and that this usage will spawn a myriad of as yet unspecified applications. The skeptics have pointed to the expense and difficulties of the technology and have forecast its early demise except in a few specialized areas where small size is essential.

We see, in the near term, a mix of monolithic and hybrid circuits. Some systems will be completely monolithic or completely hybrid, but a large percentage of them will consist of monolithic IC's in an MIC hybrid environment. The monlithic IC's could then be treated as higher order components (let's all promise not to call them "Superchips") which could be designed into conventional circuitry, obtaining the best that each technology has to offer.

The Hughes Radar Systems Group has recently completed a Solid State Aperture Module program for the Air Force (F33615-79-C-1782) for which they designed and fabricated 80 hybrid X-band T/R modules. Meticulous cost records were kept and estimates were made for fabricating large numbers of these modules. Comparisons of these costs to estimates of monolithic IC costs provide some interesting insights into the types of monolithic circuits which will prove to be economically feasible.

The module elements to be examined here are the power amplifier, low-noise amplifier, phase shifter, and T/R switch. Not included here are other circuits which are obvious candidates for monolithic implementations, such as 0-5 GHz signal processing chips and MM-wave IC's. The costs incurred include those for purchased parts and the labor associated with fabrication, assembly,

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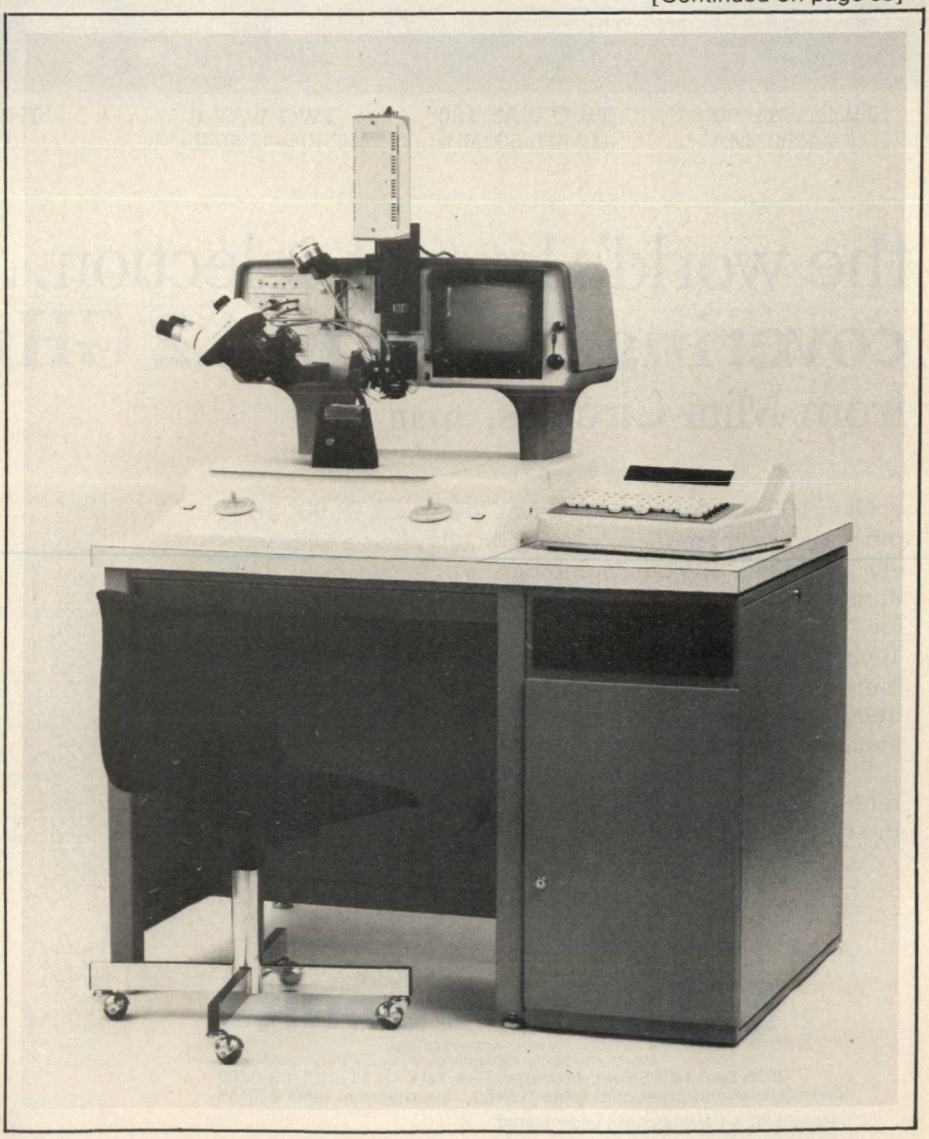

Fig. 1 Hughes 2460 automatic wire bonder with pattern recognition.

tuning, and test of the sub-modules. The main cost driver is the power amplifier, a 4-stage, 2.5 watt amplifier which accounts for 49% of the total hybrid module cost. An additional 20% of the cost was shared among the low-noise amplifier, phase shifter, and T/R switches.

Obviously, the most favorable cost impact of monolithic circuitry would occur in the power and low noise amplifier which accounts for about 60% of the cost presently experienced in our module design. It should be noted that the sub-module assembly, tuning and test were not done in a volume production environment and thus the mode of operation was relatively inefficient and manpower intensive.

In the future, however, significant cost reduction of hybrid circuits is expected. Such cost reduction will result from the implementation of automated assembly and test procedures. Along with reduced costs, the uniformity of discrete FET's will improve so that little or no tuning will be required at the assembly and test level. All of these trends will result in substantial cost savings for the hybrid module.

Examples of technologies which will lower hybrid costs include:

- Automated wirebonding machines with pattern recognition systems (See Figure 1) will accurately position and bond one mil diameter gold wire to two mil pads at a rate of one per second. Lead dress, and therefore, inductance is uniform from device to device, minimizing a major cause of variation and expense in hybrid circuitry.
- Thick film hybrid circuitry has developed rapidly in the past several years. Circuits can be fabricated on alumina with low-loss gold conductors ground planes, via holes, M-O-M capacitors and resistors all screened and fired on in an inexpensive batch manner. Estimates for a ½ × ½ substrate, batch fabricated on a 3 × 3 alumina substrate, with a variety of the above-mentioned components is $1.50 for material and labor with a yield of 90% in large quantities. If the ± 1 mil variation on conductors and spaces can be tolerated, this should prove to be an attractive medium for hybrid circuits.
- GaAs material and process technology appears to be, finally, maturing and recent lots of low-noise and power FET's have shown remarkably consistent parameters. This bodes well for both monolithic and hybrid costs.

The hybrid costs in the following graphs are based on our documented costs, appropriately modified to account for new technology and high volume. Monolithic costs, on the other hand, are somewhat more nebulous. A variety of monolithic amplifiers, phase shifters, and T/R switches are under development and have been produced with surprisingly good yields. They were fabricated, however, in a non-automated manner, one wafer at a time with considerable care and patience at each processing step. This is a long way from the automated processing which must be developed for monolithic IC's to attain their full potential.

In order to compute the monolithic circuit cost, a number of assumptions have been made.

These assumptions include:

- Fabrication of the monolithic circuitry is carried out in a production environment with some automated wafer handling.
- Production lots consist of three 2″ diameter wafers.
- The overall passive component yield is 90%.
- Each monolithic circuit is packaged in a hermetically sealed housing and the cost for the packaging materials and labor, including test, is estimated to be 50 dollars. Based on these assumptions, the cost of each type of monolithic circuit is calculated and a comparison of the cost between the monolithic circuit and the corresponding hybrid MIC is made.
- Physical and/or electrical defects of the active elements are randomly distributed over the wafers.

This last assumption is based on Boltzmann statistics and is the most commonly used, giving a yield which is exponentially dependent on gate periphery, W:

$$y = k_1 e^{-K_2 W}$$

where K_1 is related to the passive circuit yield and K_2 to the yield per unit gate length. Price[2] has shown that if the defects are due to some identifiable set of mechanisms, such as critical processing steps, Bose-Einstein statistics should be used giving a yield of:

$$y = \left(\frac{1}{1 + P_1 A}\right)\left(\frac{1}{1 + P_2 A}\right)\ldots$$

where P_1 refers to separate defect causing mechanisms and A is the chip area. This produces a much more optimistic view of yield than Boltzmann statistics as shown in Figure 2, where yield is plotted as a function of the number of devices per chip when the yield of a single device is 50 percent. The Bose-Einstein curve is plotted for a single defect causing mechanism. Preliminary monolithic IC and FET yield data at Hughes and in the literature is consistently above the more optimistic curve.

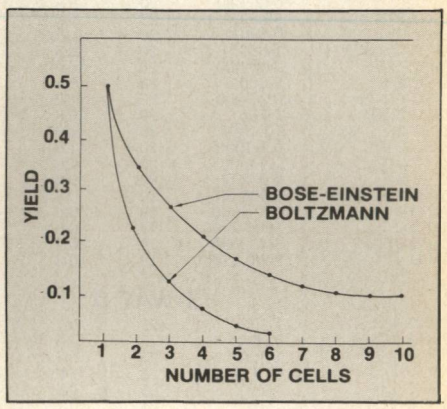

Fig. 2 Yield of multicell circuit assuming single cell yield of 50%.

The yield numbers factored into the following comparisons are based on Boltzmann statistics.

Power Amplifier

The amplifier consists of three 2400 μm FET's, one each 900 μm FET's, and the total gate width is thus 8.4 mm. In order to make a fair comparison of the cost of a monolithic amplifier with the corresponding hybrid MIC amplifier, the cost of the discrete FET's used for the hybrid amplifier is calculated as a function of the yield. The total manufacturing cost of the hybrid power amplifier is then computed as a function of the discrete FET yield. The gate length of the monolithic FET is assumed to be 0.8 to 0.9 μm, the same as that of the discrete device. Therefore, the same device yields are expected for the discrete and monolithic FET's with the same total gate width.

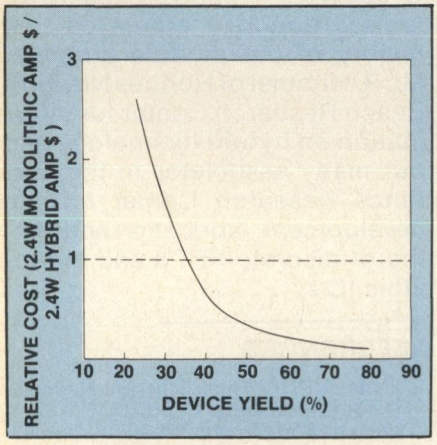

Fig. 3 Device yield of 2.4mm power FET with a gate width of 0.8 μm

Since the total gate width of the monolithic power amplifier is 8.4 mm and hence 3.5 times larger than that of the 2.4 mm discrete FET, the yield of the FET's in the monolithic amplifier is reduced to $Y^{3.5}$ where Y is the functional yield of the 2.4 mm discrete FET. Assuming the pessimistic Boltzmann statistics, the relative cost of the 2.4 watt monolithic power amplifier (manufacturing cost of the 2.4 watt monolithic amplifier/ manufacturing cost of the corresponding hybrid MIC amplifier) is illustrated as a function of the 2.4 mm gate power FET yield in Figure 3. The curves indicate that the monolithic amplifier becomes less expensive than the corresponding hybrid amplifier when the 2.4 mm power FET yield exceeds 36%.

Low-noise Amplifier

This amplifier consists of two 300 μm low-noise FET's with a gate length of 0.6 to 0.7 μm. Comparison of the manufacturing cost between the monolithic amplifier and the equivalent hybrid version is made as a function of the 300 μm low-noise FET yield and the results are illustrated in Figure 4.

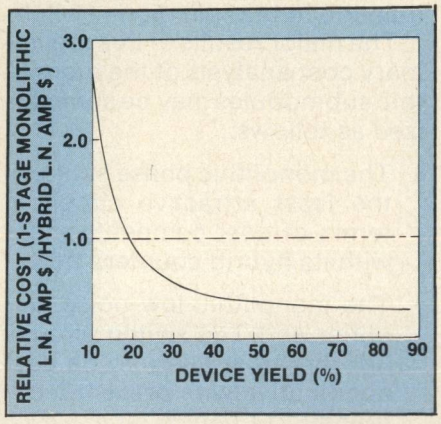

Fig. 4 Device yield of L.N. 300 μm FET with a gate length of 0.7 μm.

The assumptions are the same as those used in the case of the above power amplifier. The cost advantage of the monolithic amplifier becomes apparent when the yield of the 300 μm low-noise FET exceeds 20%. Since our current yield for the X-band 300 μm low-noise FET's is higher than this, the monolithic amplifier is already cost effective as compared with the hybrid equivalent.

— Phase Shifter

The five-bit phase shifter consists of fifteen 1.2 mm power FET's with a total gate width of 1.8 cm. We consider two approaches, one using a single chip containing 15 FET's, and the other using three single-bit (180°, 90°, and 45°) chips and a single two-bit (22.5° and 11.25°) chip. The latter case offers benefit of higher yield. The hybrid phase shifter used for cost comparison is one currently used in the Solid State Aperture Module Development Program and consists of PIN diode switched line elements.

The manufacturing cost comparison is made as a function of the yield of the 1.2 mm power FET with a gate length of 1 to 1.2 μm.

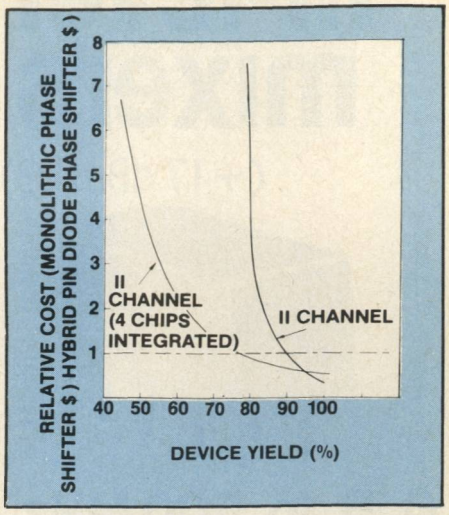

Fig 5 Device yield of 1.2mm power FET with a gate length of 1.0~1.2 μm.

The result is illustrated in Figure 5 for the one-chip and four-chip configurations. The cost advantage of the monolithic FET phase shifter does not appear until the 1.2 mm power FET yield reaches above 75% for the four-separate-chip configuration and above 90% for the single-chip configuration. The monolithic FET phase shifter is thus somewhat unattractive on the basis of this cost comparison.

— T/R Switch

The switch consists of two 1.2 mm power FET's and the total gate width is thus 2.4 mm. The manufacturing cost of the monolithic FET T/R switch is compared with that of the pin diode used for the current Solid State Aperture Module Development Program.

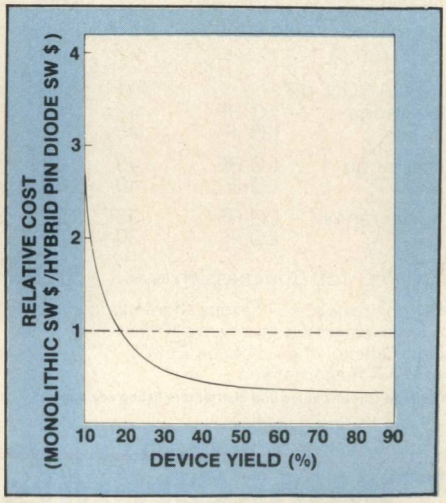

Fig. 6 Device yield of 1200 μm FET with a 1-1.2 μm gate length.

[Continued on page 100]

[From page 99] **HYBRID vs. MONOLITHIC**

The cost comparison is made as a function of the 1.2 mm power FET yield, and the result is illustrated in Figure 6. The gate length of the FET is 1 to 1.2 μm and thus reasonably good yield is expected. The results are similar to those of the low-noise amplifier analysis. When the yield of the 1.2 mm FET exceeds 20%, the monolithic T/R switch becomes less expensive than the hybrid pin diode switch.

The major results of this preliminary cost analysis of the monolithic submodules may be summarized as follows:

- The monolithic phase shifter is the least attractive circuit in terms of cost competitiveness with its hybrid counterpart.
- The monolithic low-noise amplifier and T/R switch circuits are the most likely to be cost competitive with present technology.
- The cost of the power amplifier, which represents a major portion of the module cost, will be reduced by monolithic circuitry when discrete power FET yields exceed approximately 40%.

Summary and Conclusions

A realistic study was undertaken to evaluate the relative costs of hybrid vs. monolithic components for an X-band phased array application. Cost breakdowns of hybrid module fabrication, tempered with new technology and high volume production tools were compared to monolithic IC cost calculated from existent data and projected GaAs production costs. IC yields were conservatively estimated from extrapolations of discrete FET yield based on Boltzmann statistics.

We fully realize the many approximations and guesses involved and there is room for constructive arguments over any of them. This is an ongoing, continually changing study as new data is obtained, but we have reached some tentative conclusions. Multistage low noise amplifiers are cost competitive with hybrid circuitry using today's monolithic technology. One watt X-band power amplifiers require more refinement before they will be cheaper than hybrid components. Hughes is committed to the development of these amplifiers and is considering small scale production for a variety of system applications.

A final conclusion is that hybrid technology is not a dying art. Optimal systems in the near future will very likely use combinations of hybrid and monolithic circuitry. A prime candidate for this is a high power amplifier consisting of multiple medium power monolithic amplifiers and hybrid power combiners.

Acknowledgements

The authors wish to acknowledge the contributions of Dr. E. Gregory of Hughes Radar Systems Group for the detailed cost history of the module program, Mr. R. Himmel of Hughes Newport Beach Research Center for information on hybrid technology and our many associates in the Torrance Research Center for the development, fabrication and testing of discrete FET's and monolithic IC's.

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Monolithic GaAs FET Low-Noise Amplifiers for X-Band Applications

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Introduction

For low-noise amplification at X-band, hybrid GaAs FET MICs have become widely used. For certain high volume applications, however, hybrid components cannot meet the cost, size, and weight requirements. Two such applications appear to be phased-array radar systems and satellite television receive only (TVRO) systems. Receive amplifiers for these applications require noise figures in the 2 to 4 dB range with 20 to 30 dB gain over 500 to 1000 MHz bandwidths at various frequencies from 9 to 13 GHz.

Monolithic microwave components fabricated on GaAs substrates provide the opportunity to meet and exceed hybrid microwave amplifier performance with greatly reduced cost, size, and weight. Advances in monolithic microwave integrated circuit (MMIC) technology have produced significant improvements in component accuracy and repeatability, allowing the circuit designer to design more complex circuits in less space with a greater degree of confidence. This paper describes the design, fabrication and performance of X-band monolithic low noise amplifiers.

Monolithic Amplifier Design

Figure 1 is a photograph of a three-stage monolithic LNA which has 3.1 dB noise figure with 26 dB gain at 10.5 GHz. Amplification is provided by three identical 300 μm gate-width, 0.5 μm gate-length FETs operated in a common-source configuration. The circuits are designed to match to 50 Ω on the input and output.

The design of the amplifier was based on data obtained from experimental characterization of discrete low noise GaAs FETs. S-parameters and optimum noise match were measured at minimum noise figure bias conditions on discrete FETs which exhibited good noise figure ($\approx$ 2 dB) and gain ($\approx$ 10 dB) performance at 10 GHz. The input matching circuit presents the optimum source impedance, or noise match, to the first stage of the amplifier to minimize noise figure. Succeeding stages incorporate matching cir-

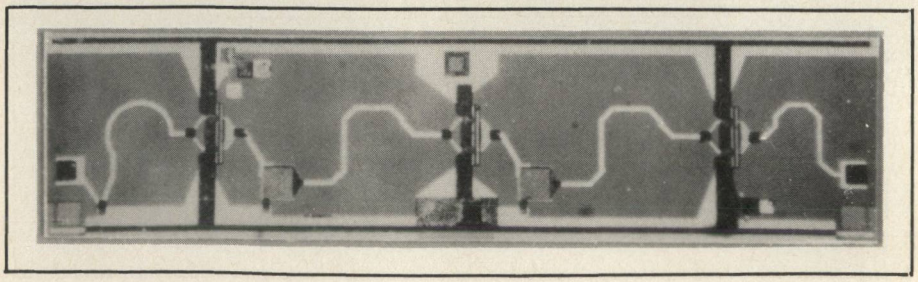

Fig. 1 3-stage monolithic common-source LNA chip.

cuits to maximize gain over the desired bandwidth.

A schematic diagram of the monolithic amplifier is shown in Figure 2. Impedance matching on the monolithic chip employs a quasi-lumped-element approach. To simplify the preliminary design of the matching circuits, a series inductor, shunt capacitor, series inductor configuration was used for the input and interstage circuits. The output stage required only a series inductor to match the FET to 50 Ω at 10 GHz. To optimize the circuit elements, COMPACT, a computer-aided analysis and optimization program, was used. The inductors were modeled as distributed high impedance (Z_o = 90 Ω) transmission lines (w/h ratio of 0.125 for GaAs).

Assuming that conductor loss is the dominant loss mechanism in the transmission lines, a loss factor of 0.25 dB/cm was used in the design[1]. The shunt capacitors and series dc-blocking capacitors were modeled as lumped elements with associated Qs dependent on the capacitance. Qs at X-band ranged from 30 for the series blocking capacitors (5 pF) to 50 for the shunt matching capacitors (< 0.5 pF)[2]. Parallel-plate type shunt capacitors were chosen to implement monolithically because of their small size and freedom from the radiation and end effects characteristic of distributed open-circuited stubs. Because the actual monolithic integration of the matching circuits involves only two photomask levels, independent of the device geometries, circuit revisions can be made easily to optimize performance. Predicted gain of the 3-stage amplifier is shown in Figure 2.

GaAs FET Design

FETs used in the monolithic LNA are 0.5 μm by 300 μm Ti/Pt/Au gate devices in a "π-gate" configuration with two feed points to the 300 μm gate stripe. As shown in Figure 3, gold-plated air bridges are used to interconnect the source regions to an expanded metallized region extending to the edge of the chip. Gates are defined by e-beam lithography for high yield and gate uniformity over large wafer sizes.

Individual FETs were scribed out of amplifier chips from the same wafer as the amplifier results being reported here. These devices have typical noise figures of 2.5 dB with 8 dB associated gain. Transconductance at low noise bias is 40 mS.

Processing

Starting material for the monolithic LNA consists of a Cr-doped GaAs substrate with a high resistivity buffer layer 1-2 μm thick and an anodically thinned n-layer doped near 3×10^{17} cm^{-3}. Epitaxial layers were deposited by conventional VPE.

The monolithic LNA was fabricated using both mesa etching and unannealed boron implantation to define the FET active areas. This procedure ensures that no parasitic buffer layer capacitance will degrade circuit performance. Gold-germanium nickel ohmic contacts were formed by conventional evaporation and lift-off. Titanium platinum-gold FET gates were defined by e-beam lithography. First level metallization (inductors and capacitor bottom plates) is 1.6 μm thick Ti/Au. Plasma deposited Si_3N_4 is used as the capacitor dielectric and to passivate and stabilize the FETs. Capacitor top plates are evaporated Ti/Au followed by plated gold. Capacitance values measured are within a few percent of the design goals. The inductors and capacitors are defined by two rather simple photomasks which can be rapidly changed using e-beam mask making. After lapping to the desired substrate thickness (0.2 mm for the current design) the backside is metallized, and the wafer is sawed into individual circuits.

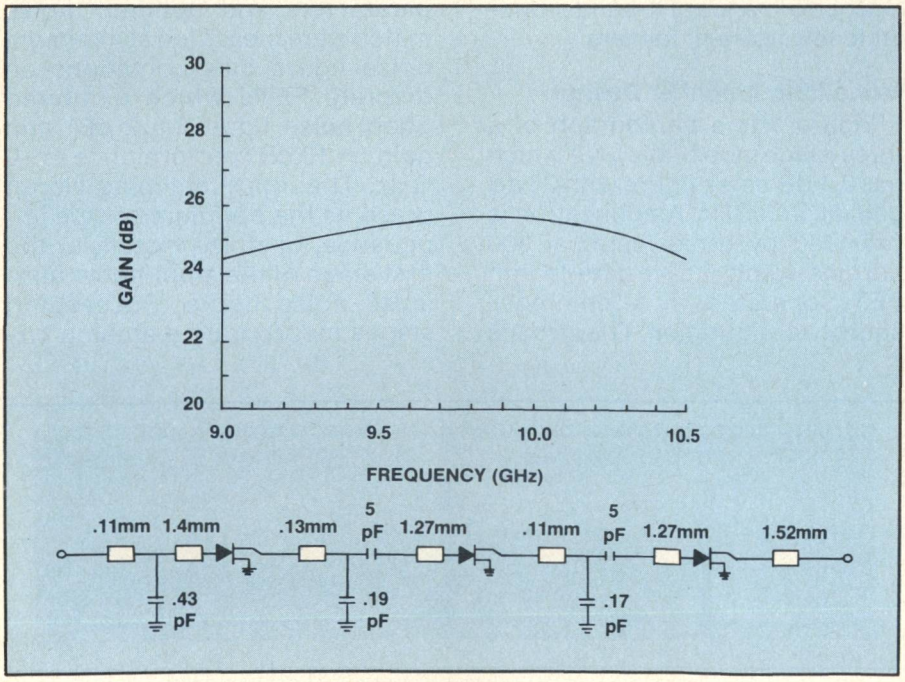

Fig. 2 Circuit schematic and computer-predicted gain response of monolithic three-stage low noise amplifier.

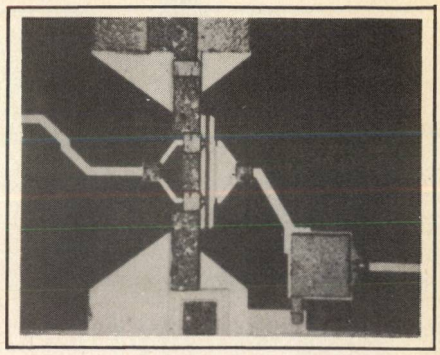

Fig. 3 A monolithic π-gate FET.

Amplifier Performance

Figure 4 is a plot of the amplifier gain and noise figure. As shown, the noise figure is 3.1 dB and the gain is 26 dB at 10.5 GHz. From 10 to 11 GHz, noise figure is below 3.5 dB and gain is above 23 dB. Input VSWR (Figure 5) is 2:1 at 10.5 GHz but degrades badly over a moderate bandwidth.

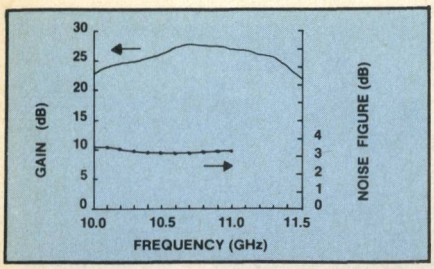

Fig. 4 Noise figure and gain for monolithic 3-stage CS low noise amplifier.

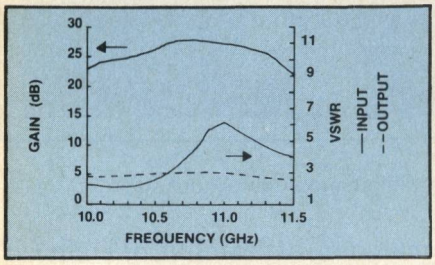

Fig. 5 Gain and VSWR for monolithic 3-stage CS low noise amplifier.

The chip, shown in Figure 1, is 1 mm × 4 mm × 0.2 mm in size. For microwave testing, the chip is mounted on a gold-plated copper carrier with SnAg solder. RF input and output connections are made with fifty-ohm microstrip on alumina ceramic. Each stage is biased with a drain-source voltage of 4 V and operates at approximately 15 mA drain-source current. Bias voltages to the gates and drains are provided through external high-impedance, low-impedance rf chokes.

Monolithic 3 dB Hybrids

Low-noise amplifiers, such as the one described in the proceeding section, do not provide a good input match because the matching network must be designed to provide the optimum source impedance for minimum noise to the input common-source FET. As a result, the input VSWR may not be suitable for many applications. A pair of 3 dB hybrids (Lange couplers) and two similar amplifiers are commonly used in hybrid MICs to improve input VSWR with a small penalty in noise figure. This balanced amplifier approach is compatible with monolithic processing; whereas ferrite isolators, which can also be used to reduce input VSWR, have not been demonstrated in GaAs MMICs.

Monolithic Lange couplers on GaAs have been demonstrated[3,4]. Loss is approximately 0.5 dB at X-band. The TI coupler[3], is a four-strip interdigitated microstrip coupler designed for use in balanced configurations which require the half-power quadrature phase outputs to be on the same side of the coupling region. The structure features air bridges to interconnect the appropriate coupling strips, allowing it to be fully compatible with the monolithic process steps of the active devices. Employing 0.2 mm thick GaAs (ε_r = 12.9), the conductor width-to-substrate-height (w/h) ratio is 0.056 and the spacing (between conductors)-to-substrate-height ratio (s/h) is 0.06.

This design results in lines and spaces of 11.4 and 12 μm in width, respectively, which can be accurately produced in MMIC fabrication. Input and output impedances are 50 Ω. The Lange coupler was fabricated on a 2.4 mm × 4.2 mm × 0.20 mm GaAs chip. Dimensions of the coupler itself are 0.11 mm × 3.2 mm.

A fully monolithic balanced amplifier would consist of two amplifiers of the type shown in Figure 1 and two 3 dB hybrids on a single GaAs chip. The total chip size is expected to range from 3 mm × 3 mm to 4.5 mm × 4.5 mm (9 to 20 mm^2) depending on whether folded couplers are used and on the complexity of the on-chip bias circuitry. Noise figures under 3.5 dB will be achieved with amplifiers similar to that of Figure 1.

New Directions: Monolithic LNA With Common-Gate Input

More recently, an X-band monolithic 3-stage LNA employing a common-gate FET at the input has been developed at Texas Instruments. The common-gate FET, used for active matching, permits single-ended operation by providing low input VSWR and low noise figure simultaneously. A 3.8 dB noise figure, 16 dB gain and an input VSWR of 1.8:1 has been achieved at 10 GHz. This amplifier, shown in Figure 6, is stable for all input and output load conditions. All matching and bias circuitry are implemented monolithically on the chip. Each stage employs a 300 μm gate-width FET with gold-plated air bridges to minimize and control grounding parasitics. Dimensions of the chip

[Continued on page 106]

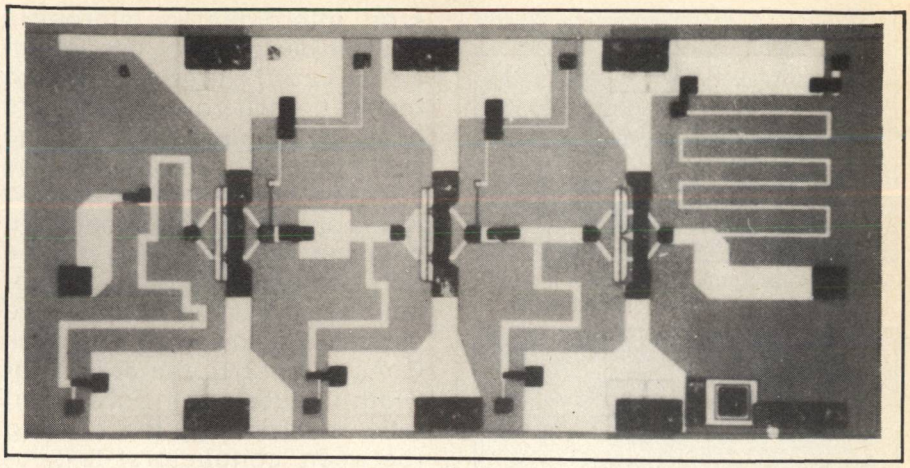

Fig. 6 Monolithic low-noise amplifier with common-gate input stage.

are 1.3 mm × 2.5 mm and 0.15 mm.

The common-gate-input circuit design makes use of extensive device modeling and CAD. The device model was constructed based on dc and rf measurements of a device similar to that used on the monolithic circuit. The device transconductance g_m, gate resistance R_g, and source resistance R_s are measured on a curve tracer or with an automatic probe station. S-parameters are measured across a broadband of frequencies at the desired operating bias condition and an equivalent circuit model is obtained with an optimization routine on COMPACT. This model can then be used for amplifier design, stability analysis, and scaling of device gate-width or gate-length, if desired.

In addition, SPICE2 is used to obtain an estimate of amplifier noise figure based on this same device model. As in the common-source LNA design, inductors are modeled as distributed high-impedance transmission lines, and shunt capacitors and series dc-blocking capacitors are modeled as lumped elements with associated Qs dependent on the capacitance.

Following the above FET and passive circuit element modeling, circuit optimization was carried out in a conventional way using COMPACT. The resultant monolithic low noise amplifier design is expected to provide good input VSWR and excellent noise figure simultaneously. The LNA employs a common-gate FET for active matching at the input, operated at an optimum transconductance to achieve low noise figure. The device is integrated monolithically on a GaAs substrate to achieve tighter control of circuit and device parasitics than can be achieved with a hybrid (discrete FET) implementation. Proper impedance loading at the drain of the FET yields an input impedance of 50 Ω over a specific bandwidth. The determination of this load impedance and its effect on gain, bandwidth, and noise figure is done with the aid of a computer. This loading technique can be extended to achieve other input impedances as may be required for specific system applications. The performance tradeoff involved in using this procedure is bandwidth versus noise figure.

An initial process lot of the common-gate input LNAs has shown 3.8 dB noise figure, 16 dB gain and an input VSWR of 1.8:1 at 10 GHz. Computer modeling had predicted < 3 dB noise figure with better gain and noise figure. Subsequent characterization of FETs removed from these monolithic circuits revealed that their parameters did not fit the model used; therefore a circuit redesign will be required. Nonetheless, the VSWR obtained over a 10% bandwidth in this initial attempt was much superior to what can be obtained by a common-source amplifier such as discussed above at similar values of noise figure.

This is the first demonstration of common-gate active matching with a high device transconduc-

tance to achieve both low input VSWR and low noise figure. For bandwidths on the order of 10-30%, this design technique allows single-ended performance without degrading noise figure. For most radar and satellite receiver applications only 10-20% bandwidths are required, thus giving an excellent opportunity to use single-ended LNAs with good input VSWRs and low noise figures. The FET used for active matching occupies less GaAs real estate than a passive matching circuit (distributed transmission lines and capacitors) as might be used in a conventional common-source input LNA, and the single-ended amplifier clearly occupies less space and consumes less power than the balanced amplifier.

Conclusions

Noise figures under 4 dB have been shown to be possible with good input match and high gain using GaAs MMICs of either the balanced common-source amplifier approach or the common-gate input active matching approach. As minor process and circuit design improvements are made, 3 dB noise figures are anticipated. Ultra-low amplifier noise figures around 2 dB will be achieved with more extensive process and materials development which is required to integrate materials and gate formation techniques used for ultra-low noise discrete devices in monolithic form.

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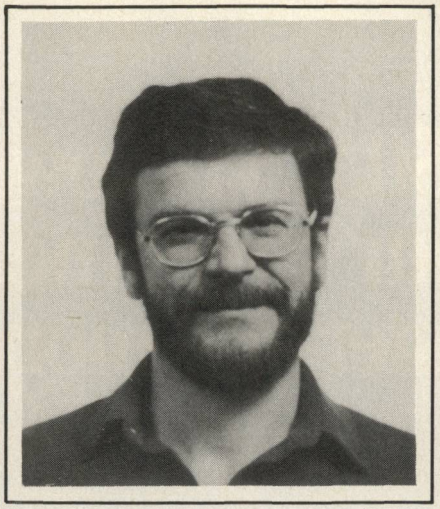

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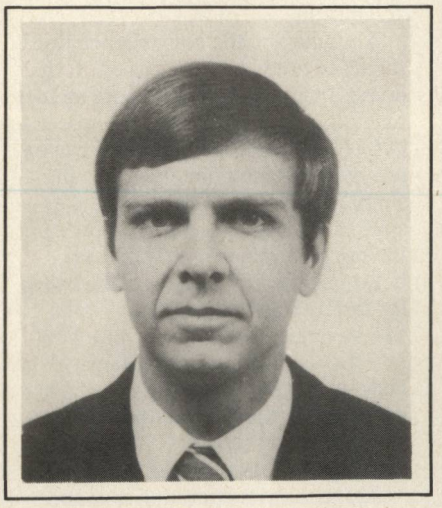

Randall E. Lehmann, *received his B.S. and M.S. degrees in electrical engineering from the University of Illinois in 1974 and 1976, respectively. Since joining Texas Instruments in 1976, he has been engaged in device characterization and modelling of GaAs FETs and IMPATT diodes for microwave and millimeter wave applications. He is currently responsible for the design and development of monolithic low noise FET amplifiers for use in satellite and airborne phased array radar systems.* ■

Flip-Chip BeO Technology Applied to GaAs Active Aperture Radars

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Introduction

Flip-chip GaAs FET technology offers an attractive method to build production volumes of microwave power amplifiers, particularly in cases where high power, low cost, and small size are required. The key technology feature which makes this possible is successful mounting of discrete GaAs FETs on BeO substrates on which the passive circuits relating to amplifier designs are photodeposited.

This paper will show the implementation of this technology leading to the production of two hundred X-band units in which multistage amplifiers were integrated on single miniature BeO substrates. These units are now being integrated into miniature packaged driver/power amplifiers for an experimental phased array system. The program has been pursued to develop a common design technology which can be applied to many circuit applications. The bandwidth capability is essentially octave with common source configuration, and potentially decade using other circuit layouts.

Present hybrid or monolithic techniques have not yet proven capable of simultaneously meeting the cost and performance requirements of today's phased array transmitter designs. Typical hybrid approaches require the alignment of several elements, including circuit boards, on a carrier. The FET devices must be upright mounted on a metal pedestal with parasitic bond wires making circuit interconnections. The assembly tolerances and labor intensive operations result in an expensive unit. Repeatability at X-band frequencies is also a problem. Monolithic devices are presently limited by non-optimal thermal performance at power levels of one watt or higher. Yield is presently also a problem, since large amounts of expensive GaAs are used for passive circuitry. In addition, present processing technology limits matching circuit topologies and therefore matching circuit flexibility.

By flip-chip mounting GaAs FET pellets directly onto BeO matching substrates, many of the best properties of both technologies are combined. This approach is particularly useful for medium to large production quantities. Power levels in excess of one watt have been achieved at a very low cost, with excellent thermal performance. Octave bandwidth capabilities have been demonstrated. This approach has proven practical using present day technology, its high power potential is state-of-the-art and X-band MICs using this technology are within a factor of two in size of MMICs.

BeO — The Choice Substrate for Miniature GaAs MICs

Thermal dissipation is one of the most critical factors for minia-

TABLE I
PROPERTIES OF BeO AND GaAs

	99.5% BeO	GaAs
Relative Dielectric Constant	6.6	12.6[5]
Loss Tangent @ 10 GHz	0.004	<0.0005[5]
Thermal Conductivity (Wcm°C)	2.5	0.44
Coefficient of Thermal Expansion	9×10^{-6}	5.9×10^{-6}

ture power amplifiers. In situations in which it is desirable to mount an active device on an insulator, beryllium oxide (BeO) is an outstanding choice. Polycrystalline BeO has a thermal conductivity of about 2.5W/cm°C. It is particularly well suited as a substrate for GaAs due to the close thermal expansion coefficient match between the two materials. The properties of BeO and GaAs are summarized in Table I.

BOMICs — Beo Microwave Integrated Circuits

The major advantages of flip-chip mounting GaAs MESFETs on BeO are:

- parasitic reduction
- low thermal resistance
- reproducible non-critical assembly
- potentially lower amplifier module cost.

In this approach, metallization patterns, which include both RF circuitry and mounting areas for the source, gate, and drain bumps of the FET die, are photolithographically defined on the BeO. The FET die is then flip-mounted onto the circuit board, as illustrated in Figure 1, using a split optic system to achieve accurate device/circuit registration. Note that bond wires to the FET pellet are not required — a key factor of this technology. Because the typical input resistance of a 1W GaAs FET is quite low, about 2.8 ohms, very small errors in bond wire length, spacing or loop height translate to large reactance changes, compromising performance. Bond wire inductances are used only at impedance levels where small errors can be tolerated. Grounds close to the FET pellet are achieved using wraparound metallizations and/or through holes.

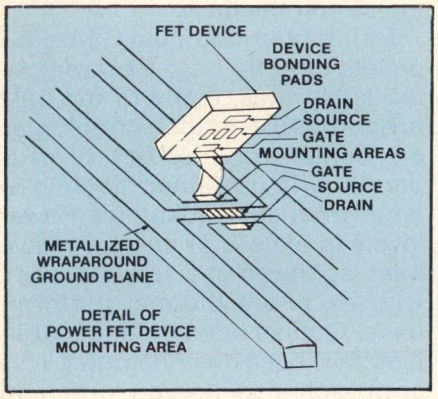


Fig. 1 Sketch illustrating flip-chip mounting of a FET pellet on metallized BeO circuit patterns. Note the absence of bond wires.

Flip-chip mounting on high thermal conductivity BeO results in excellent thermal performance. As shown in Figure 2, the heat source in a power FET chip is essentially a line source. Most of the temperature drop is across the heat spreading region directly adjacent to the heat generation region. Since thermal spreading resistance varies inversely with thermal conductivity, heat extraction in a flip-chip/BeO hybrid circuit can be more efficient than through GaAs substrates of reasonable thicknesses.

It has been shown[2] that wafer thicknesses of 30μm for upright devices are needed to achieve a thermal performance equivalent to that of flip-chip designs. However, processing wafers to such thicknesses is difficult and thermal expansion mismatches between GaAs and high thermal conductivity metals has been reported to cause cracking of large discrete GaAs power FET devices[3]. Furthermore, when matching circuits are incorporated on GaAs a tradeoff must be made between substrate thickness and transmission line loss[4], particularly for thicknesses under 100μm. Mounting a 200μm thick GaAs die onto 0.015" BeO results in a sturdy structure with high thermal conductivity.

The initial hybrid modules for the phased array demonstration project were fabricated on thick film screened BeO. The thermal resistance of 1 watt units measured by hot spot IR scanning techniques[6] is typically 22°C/W. Prototype units built using thin film Ti-Pt-Au metallization achieved 15.2°C/W. With a baseplate temperature of 50°C, the channel temperature for such units is less than 100°C under DC bias. Using life test data for MSC devices[1], a MTTF of well over 10^7 hours is predicted. Since the heat sinking properties of this mounting technique are independent of the electrical connections, many different topologies (such as grounded gate, or single bias operation) are available to the circuit designer.

Design Concepts and BOMIC Performance

Two amplifier blocks were developed using flip-chip BeO technology for the active aperture antenna: a single stage power amplifier, and a two-stage driver amplifier. Both blocks use standard devices and models were made for each device from available data bases to facilitate computer-aided circuit design. The matching circuits for the one watt block are of simple low pass filter form. The two-stage driver amplifier uses band pass filter elements to achieve a wide band match between the drain of the input FET and the gate of the output FET. Both amplifier blocks are matched to 25 ohms to reduce losses and increase bandwidth.

Impedance matching is accomplished using a combination of lumped and distributed line matching elements. Transmission lines and stubs are printed on the substrate. One mil diameter gold bond wires may be used as induc-

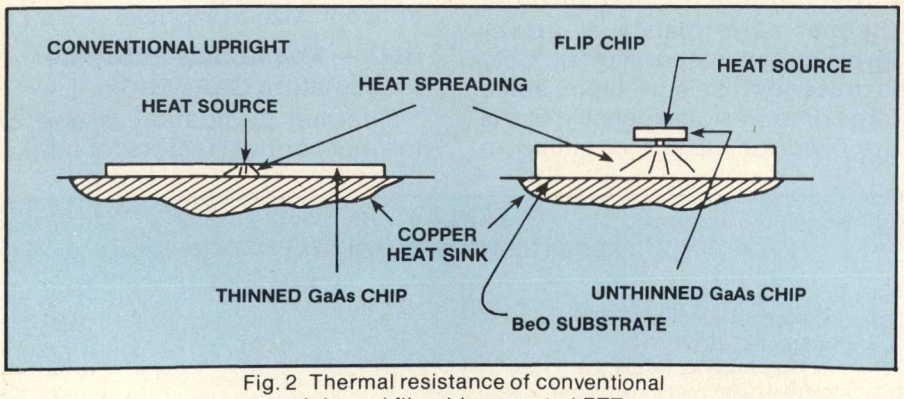
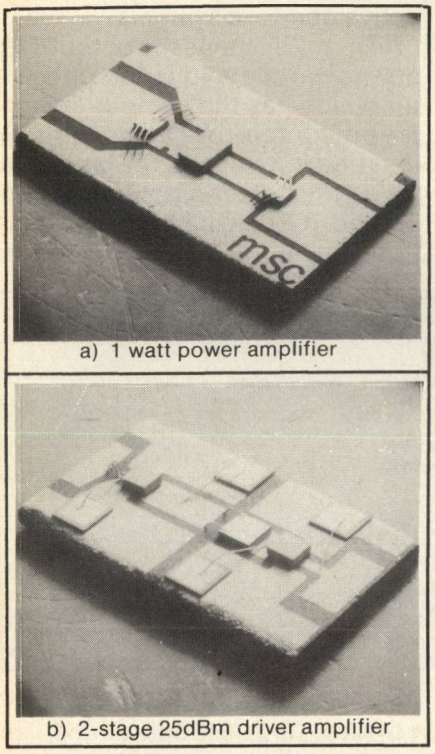


Fig. 2 Thermal resistance of conventional upright and flip-chip mounted FETs.

tive matching elements. High relative dielectric constant capacitors are used in both shunt and series connections allowing a wide range of capacitance values, difficult to obtain using other techniques. RF bias chokes are made with bond wires and MOS capacitors and fit entirely on the circuit board. The resulting substrate has an area comparable to an MMIC of similar power output capability.

The stages measure 0.150 x 0.250 in. and are shown in Figure 3. The power stage is rated at



a) 1 watt power amplifier

b) 2-stage 25dBm driver amplifier

Fig. 3 Scanning electron photographs of the BOMIC amplifiers. The input is at the upper left hand corner in each case. Actual size is 0.15 x 0.25 inches.

+29dBm output with 5dB gain while the driver delivers in excess of 12dB gain. Typical power and gain performance for each unit are shown in Figure 4. Both exhibit a bandwidth exceeding 1 GHz centered at 9.5 GHz. The transfer phase for a sampling of 5 power amplifiers is shown in Figure 5.

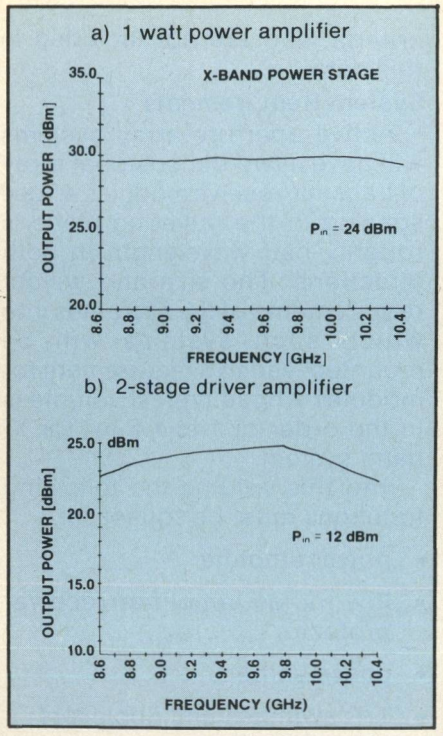


Fig. 4 Output power versus frequency for the two amplifier modules of Figure 3. The design bandwidth was 9.1 to 9.9 GHz.

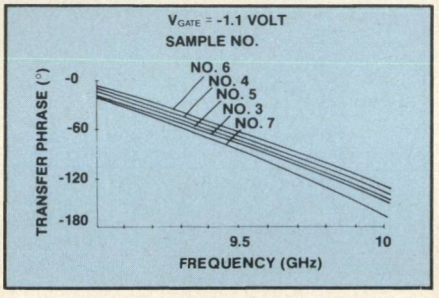


Fig. 5 Transfer phase of power amplifiers.

The uniformity of phase tracking is sufficient for use in a phased array system without additional phase compensation. Similar uniformity is also achieved with the driver amplifiers.

Pilot production of over 200 amplifiers has been completed. Table 2 shows the power output distribution for 65 units from a production lot of 84 single stage amplifiers. The remaining devices were rejected on DC, RF, or visual

[Continued on page 112]

TABLE II
PERFORMANCE OF 65 ONE-STAGE AMPLIFIER BLOCKS

Frequency (GHz)	Mean Output Power (dBm) P_{in} = +24dBm	Standard Deviation	Highest Output Power
9.1	29.29	.376	30.2
9.5	29.53	.316	30.2
9.9	29.36	.328	30.2

[From page 111] **FLIP-CHIP BeO**

criteria, and are not included in this data.

System Requirements

Active aperture array systems will have a two dimensional array of transmit/receive modules whose spacing in the radiating plane is roughly half wavelength in both directions. The size and weight requirements of the airframes into which such systems will be mounted lead to a requirement for modules whose typical volume is in the order of 1 to 1.5 in^3 for X-band system.

Into this volume the following functions must be squeezed:

- power amplifier
- low noise amplifier/receiver protector
- phase shifter
- T/R switches and duplexers
- prime power conditioning circuitry
- heat removal system
- radiating element
- manifold connector
- mechanical mounting structure
- hermetic envelope.

Studies held here and elsewhere lead to a system requirement of peak output power of about 2 watts per module at the radiating element, or about 2.4 watts at the power amplifier output, in a volume of about 0.5 in^3.

The cost objectives of the modules in production quantities are in the order of $500, after extensive cost reduction from the existing MIC technology base. Presently such MIC modules cost in the order of $5-10K in small quantities. The purchased parts cost typically is in the order of 25% of these figures, consistent with MIC total cost/parts cost ratio background experience of 4:1. This ratio reflects the large amount of test/tune operations presently required of MIC technology, and points up the need of a new technology which reduces the need of this test/tune sequence and reduces the cost-driving features of the MIC techniques, while still preserving the size and performance features necessary for active aperture systems.

In many systems the output T/R device can be a junction circulator which has the obvious advantage of no control signals with low loss and low weight (0.7 gms!). As far as the power amplifier is concerned, it would have characteristics similar to those in Table 3.

TABLE III

POWER AMPLIFIER CHARACTERISTICS

Size	**0.25" x .1" x 0.125"**
Gain	**≤25dB**
P_{out} (peak)	**2.5 watts**
Duty factor	**≤0.5**
Power-added efficiency	**≥25%**
Pulse width	**0.25 - 50 μsec**
Phase tracking	**2° over 10 MHz bands within 9-10 GHz**
MTBF	**≤25 failures/million hours**
Spurious signals	**≤80dBC @ full drive**

Items (1) through (5) are fairly obvious. Item (6) regarding pulse width indicates that the power amplifier specifications be essentially the same for CW operation because typical FET thermal time constants are a few 10's of microseconds.

Item (8) is pacing for airborne active aperture systems because of the effect on overall antenna MTBF, which should be in the order of 1000 hours. The 25 failures per 10^6 hour figure is based on reliability studies done here and elsewhere, and is related to junction temperature by Arhennius plots with activation energies in the 1.5 -1.8 ev range. Our studies indicate that 110° C is a reasonable goal for all FET junctions, and this requires individual devices with very low thermal resistance from the junction to the heat sink.

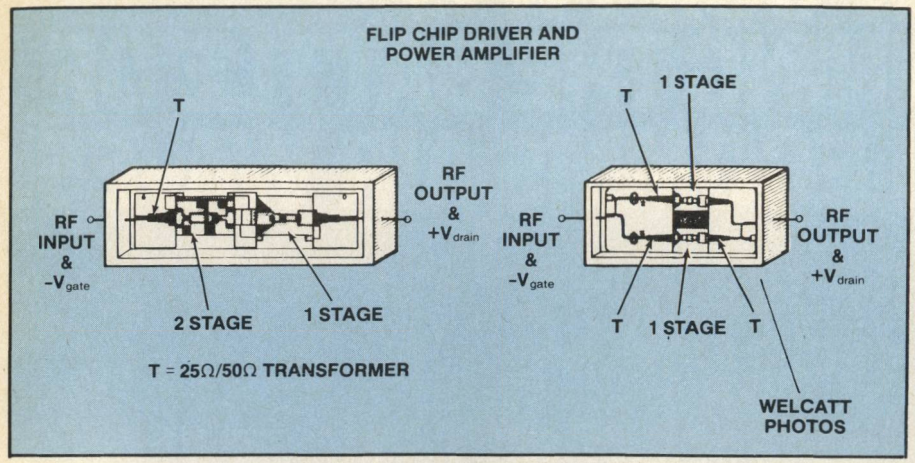


Fig. 6 Driver and power amplifier integration.

BeO Module Integration

A demonstration active aperture X-band antenna system using the modular flip-chip-on-BeO amplifiers described previously is under development. The two BeO modules are integrated and arranged as in Figure 6a and 6b. Each unit comprises a hermetic kovar package with Corning 7052 glass seals. The BeO units encased within are matched to 25 ohms, and transformers ("T" in the figures) are provided to match to the 50 ohm circuits outside of the BeO sections. The output power amplifier is balanced, using Lange couplers on Al_2O_3, though in a high production version this could all be done on BeO, with little increase in size. The BOMIC modules are currently being integrated into a 32 element demonstration phased array antenna.

Conclusion

The BOMIC concept shows great promise for high power, low cost high volume applications, particularly when the following features are needed:

- small size
- long MTBF and high reliability (due to low junction temperature)
- innovative circuit topologies (not limited to common source FETs)
- overall small packaged functional construction.

All the fabrication and processing technologies are firmly developed and in present use. Since each amplifier stage uses a standard GaAs FET die, exceptionally high wafer yields are not necessary for low unit cost. Additionally, fast design turnaround times are achievable, since the active (FET) and passive structures are fabricated independently. Finally, the flip-chip concept has other advantages including:

- The chips need not be chemically thinned. This improves chip handling yield and reduces the number of operations on GaAs.
- Much less GaAs is used for a given amplifier, reducing GaAs cost.
- No critical wire bonds are needed.

Acknowledgement

The authors wish to acknowledge the contributions made by Mr. C. Chandler in microwave measurements of the amplifiers.

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Sensitivity of EW Receivers

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Introduction

This paper can be considered as a follow-up to "Tangential Sensitivity of EW Receivers[1]." From a user's point of view, the sensitivity of an Electronic Warfare (EW) receiver is the time between false alarms and the probability of detection at a certain input power level. A method of determining these parameters has been discussed by authors such as Skolnik[2] and Swartz[3]. However, in these discussions, the radio frequency (RF) bandwidth (B_r) is close to that of the video bandwidth (B_v) (i.e., the ratio of B_r to B_v ($\gamma=B_r/B_v$) ranges from 1 to 2). In EW applications such a limited B_r to B_v range may apply only to a select group of receiver types such as the superheterodyne or the channelized receiver. In many EW applications, the ratio of B_r to B_v can vary from 1 to several thousand. For example, the Instantaneous Frequency Measurement (IFM) and crystal video receiver typically have γ values ranging from a few hundred to thousands. The operational sensitivity of receivers with high γ values here-to-for, has been a disconcerting area of investigation because of the apparent conflict between theoretical calculations and laboratory measurements. For example, calculations have shown[4] that even with false alarm rates as low as 10^{-10} a signal-to-noise ratio (S/N) of approximately -6dB can provide a probability of detection value of 90%. However, datum collected from actual receiver measurements was different from this prediction. This paper shows that the apparent conflict between the theoretical predictions and measured quantities is not a conflict at all, but rather a misinterpretation of the theory. Indeed this paper shows that theory and laboratory measurement agree quite well. Another area of concern this paper addresses is the relationship between the operational sensitivity and the tangential sensitivity. This relationship is important, since tangential sensitivity can be easily calculated for any γ and it is quite readily measured.

Background

Since this paper only tries to show the approach of the calculation, the detailed mathematics will not be presented here. However, the general approach with references will be presented here.

(1) The basic equations to generate the false alarm rate and probability of detection were given by Emerson[5]. The detailed mathematical manipulation of how to generate the curves are discussed in references 6 and 7. Reference 7 will also provide a family of curves for design applications. The general approach is as follows:

a. Define a probability density function p(E) where E is the output voltage from the video amplifier following the detector. p(E) is a function of (S/N) and γ.

b. The false alarm rate is obtained from:

$$P_{fa} = \frac{\int_{V_t}^{\infty} p(E)\Big|_{\frac{S}{N}=0} dE}{\int_{o}^{\infty} p(E)\Big|_{\frac{S}{N}=0} dE} \quad (1)$$

c. The probability of detection at a certain value of S/N is obtained from:

$$P_d = \frac{\int_{V_t}^{\infty} p(E)\Big|_{\frac{S}{N}} dE}{\int_{o}^{\infty} p(E)\Big|_{\frac{S}{N}} dE} \quad (2)$$

(2) The results derived from the above equations are independent of the properties of the detector and the noise figure of the video amplifier following it. It is assumed that the detector is a square-law device. From reference 1, it has been shown that the RF gain in front of the detector must be sufficiently high to make the sensitivity of the receiver independent of the detector and video amplifier, otherwise the tangential sensitivity of the receiver is detector/video amplifier dependent. Similar conditions will be assumed here. Specifically that:

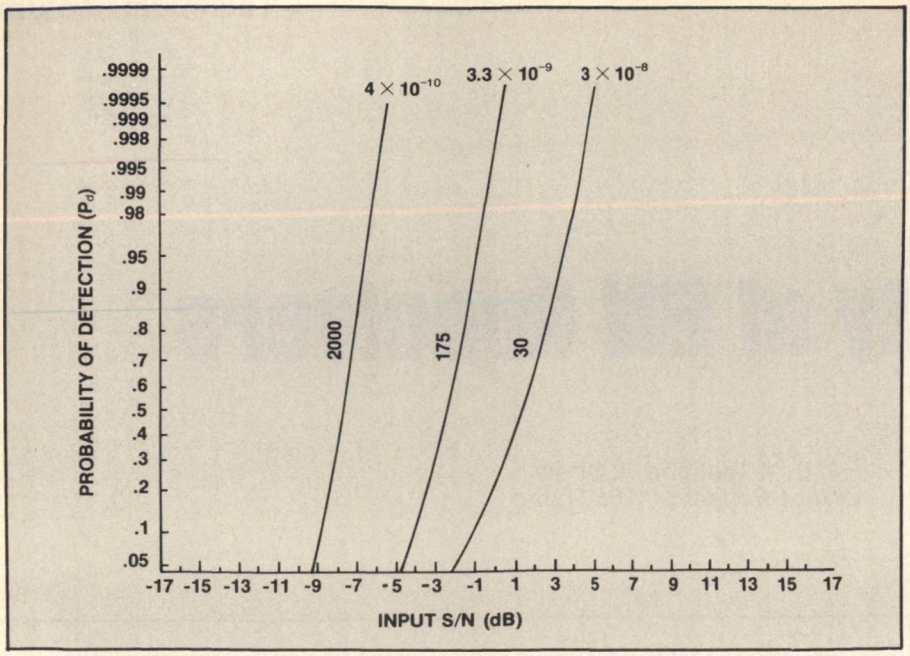

Fig. 1 Probability of detection as a function of S/N and probability of false alarm.

$$G_t > \frac{2.24}{F_t}\sqrt{\frac{A}{2\ B_r - B_v}} \qquad (3)$$

where G_t and F_t are the total gain and noise figure from the input of the receiver to the input of the diode respectively. The constant A in equation (3) is related to the diode parameter which is discussed in detail in reference 1. Condition (3) is fulfilled in most modern receiver designs.

(3) For this discussion, the three curves shown in Figure 1 were generated. These curves were generated specifically to evaluate the experimental results which will be discussed later.

Basic Approaches

The following approaches should be used to determine a receiver's sensitivity. It must be kept in mind that there is sufficient RF gain in the receiver.

(1) The operating conditions of the receiver must be specified. These include: B_r, B_v, the mean time between false alarm (T_{fa}) and probability of detection (P_d). From B_r and T_{fa}, the value of P_{fa} may be calculated through[2]

$$P_{fa} = \frac{1}{T_{fa}B_r} \qquad (4)$$

(2) From P_{fa}, P_d and $\gamma(B_r/B_v)$, the required signal-to-noise (S/N) ratio can be read from curves similar to those shown in Figure 1. It is critical to note that the S/N read is at the input of the detector. It does not represent the S/N at the input of a receiver. The input power required to produce the given P_d can be calculated from the noise figure of the receiver.

(3) The noise level at the input of the detector can be calculated as:

$$N = -114 + 10 \log B_r + F_t \text{ (dBm)} \qquad (5)$$

where -114dBm is the thermal noise floor for a 1 MHz bandwidth and B_r must be expressed in terms of MHz. The input power level P_i can be calculated as:

$$P_i = N + \frac{S}{N} \quad \text{(dBm)} \qquad (6)$$

where S/N is the value read from curves as shown in Figure 1.

Experimental Configuration

The basic experimental set-up is shown in Figure 2. Amplifiers A_1 and A_2 provide enough gain to fulfill equation (3). The 6dB pad is used to improve the matching between the two amplifiers. Three different filters were used in Figure 2, to simulate different conditions.

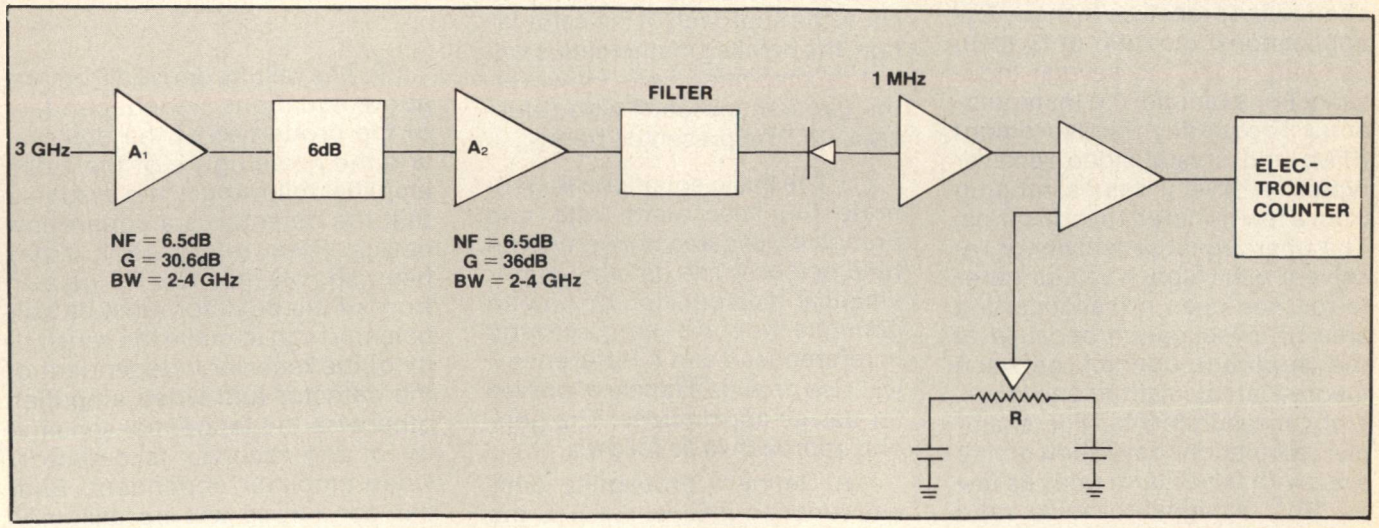

Fig. 2 Experimental set-up.

(1) In this experiment, the first step is to establish and measure the mean time between false alarms (T_{fa}). In order to accomplish this, the input of amplifier A_1 was terminated with a matched load. The resistance R is varied and at the same time the false alarm rate reading on the electronic counter is observed. The resistance is set at a level that the reading on the counter is increasing by approximately 1 per second. This is a value which is easy to read and there is no magic about it. The counter reading is recorded after 200 seconds. The T_{fa} is then calculated.

(2) The probability of detection P_d was measured by applying a 1 μs pulse with center frequency of 3 GHz (approximately the center of the filter) and pulse repetition frequency (PRF) of 1 kHz. The input signal strength is increased and frequency indication in the counter is read. A PRF of approximately 400-800 Hz is the range of interest. The measured PRF divided by the input PRF (1 kHz) is the measured value of P_d. In this measurement, there are two problems that will be discussed here.

a. The PRF is very sensitive to the input power level which can only be changed at a minimum 1dB per step. The variation of the probability of detection can be shown also from the shapes of curves in Figure 1.

b. When the counter is just starting to trigger, the PRF might be higher than 1 kHz because it has noise triggering problems too. However, increasing the input power, the counter reading will be stable and the PRF will start below 1 kHz and reaches 1 kHz by further increasing the input power.

Experimental and Calculated Results

The following three cases were obtained:

(1) The first filter used is a YIG tuned filter with a 30 MHz bandwidth and 7.1dB insertion loss. The measured false alarms are 173 in 200 seconds. The measured P_d is 0.66 at -89dBm. The calcula-

[Continued on page 120]

TABLE 1

Filter Bandwidth in MHz	Operational Sensitivity (dBm) Calculated From Ref (2)	Calculated From This Paper	Measured	Tangential Sensitivity (dBm) Calculated	Measured
30	-84.5	-91	-89	-93	-91
175	-72	-87.5	-87	-90	-88
2000	-61	-82.5	-83	-85	-84

tion is as follows; the mean time between false alarm is:

$$T_{fa} = \frac{200}{173} = 1.16 \text{ sec}$$

The probability of false alarm rate from equation (4)

$$P_{fa} = \frac{1}{T_{fa}B_r} = \frac{1}{(1.16)(30 \times 10^6)}$$

$$= 2.87 \times 10^{-8} \simeq 3 \times 10^{-8}$$

The (S/N) at the input of the detector is read from Figure 1, as approximately 1.5dB. The noise figure from the front end to the detector is $F_t \simeq 6.5$dB. Then from equations (5) and (6):

$$P_i = -114 + 10 \log B_r + F_t + S/N = -91 \text{ dBm}$$

(2) A tunable 5 section filter with $B_r = 175$ MHz and insertion loss of 1.5dB replaces to 30 MHz filter used in (1). The measured false alarm in 200 seconds was 116 and $P_d = .43$ at -87dBm:

$$T_{fa} = \frac{200}{116} = 1.72 \text{ sec}$$

$$P_{fa} = \frac{1}{(1.72)(175 \times 10^6)}$$

$$= 3.3 \times 10^{-9} \approx \times 10^{-9}$$

The corresponding S/N is:

S/N = -2.5 dB (from Figure 1)

The corresponding input power is:

$$P_i = -114 + 10 \log 175 + 6.5 - 2.5$$

$$= -87.5 \text{dBm}$$

(3) A bandpass filter from 2-4 GHz with 2dB insertion loss is used. The measured false alarm is 160 in 200 seconds and $P_d = 0.46$ at -83dBm.

$$T_{fa} = \frac{200}{160} = 1.25 \text{ sec}$$

$$P_{fa} = \frac{1}{1.25 \times 2 \times 10^9} = 4 \times 10^{-10}$$

The corresponding S/N is: -8dB (from Figure 1)
The corresponding input power is:

$$P_i = -114 + 10 \log 2000 + 6.5 - 8 = -82.5 \text{dBm}$$

In the above experiments, the value of R is adjusted after each filter is inserted. The tangential sensitivity was also calculated and measured, and the results are listed in Table 1. Calculations generated from reference (2) are also included, which are far from the measured values.

Conclusions

The measured results and the calculated results agreed surprisingly well. It seems that the mystery of the signal-to-noise ratio, at the input of a receiver to generate a certain probability of detection with a desirable false alarm in a certain time, is resolved. The signal-to-noise ratio at the input of the detector (which is specified in reference 2 and 5) is used in the calculation and it is not the signal-to-noise ratio at the input of the receiver. The signal level at the input of the receiver can be calculated from the system noise figure and bandwidth.

It is emphasized here that without the amplifiers in front of the detector, the sensitivity can never reach the -80 dBm level. Thus, the discussion is limited to noise limited case as discussed in reference 1.

The operational condition chosen was suitable for experimental measurements. It may not be suitable for a receiver to function in an electronic warfare environment, because the false alarm rate is high and probability of detection is low. It is estimated that if the input signal is 3dB stronger than the measured sensitivity, a satisfactory operational condition may be obtained. Although no theoretical relation was derived between the operational and tangential sensitivities, from the experimental results, one can see that if the input signal is approximately 5dB above the measured TSS (7dB above the calculated value), suitable operational condition should be obtained. If there is not enough gain in front of the detector, the TSS can be calculated and an operational condition can be estimated.

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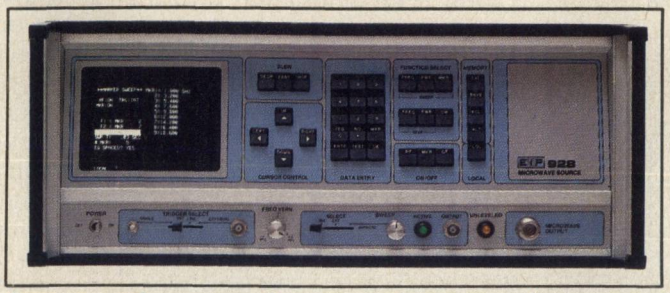
Source Power Leveling



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Introduction

In today's microwave testing environment, more precise power control is becoming increasingly important. This applies to both absolute power levels and to power flatness across the frequency band of interest. Power control is particularly important in the testing of an active device such as an amplifier, a mixer, or a detector, where any source power variations with frequency can have an adverse effect on the test. This application note describes a unique, digitally based method used in a family of microwave sources to achieve extremely flat power output over wide or narrow frequency ranges and methods for leveling the microwave source directly at the input to the device under test.

A simple diagram of the traditional method of internally or externally leveling a microwave sweeper is illustrated in Figure 1. Even the best coupler/detector combination has response variation with frequency which will be input into the sweeper's power control circuitry. An image of the coupled response variation will also appear on the coupler's output port and, hence, at the input to the device under test.

By contrast, the power level control method described here provides exceptionally level power at (or beyond) the RF output port.

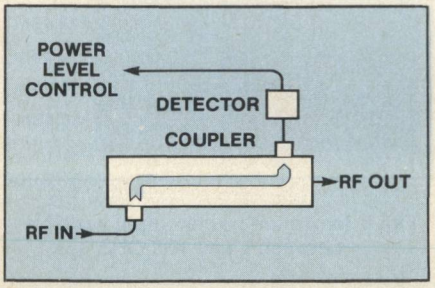


Fig. 1 Coupler/detector combination introduces variations with frequency onto the RF output.

The leveling technique corrects for any response variations with frequency introduced by the coupler/detector used within the source. The method also corrects for any slope due to variation in cable loss with frequency. The primary limit on absolute power level accuracy is the accuracy of the power meter used in the leveling process.

The Power Control System

The power control system (shown in Figure 2) consists of a power control counter, a power correction RAM, and a digital summing device. When the desired operating power is selected, the microprocessor loads a digital word representing that power level into the power

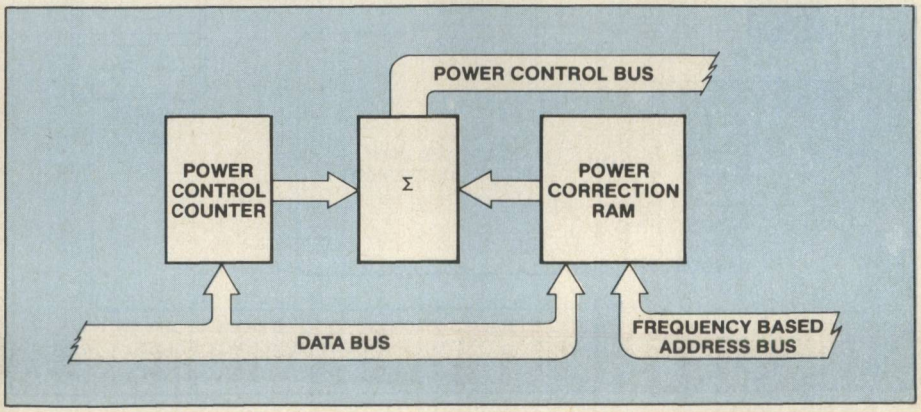


Fig. 2 Power flatness and accuracy are achieved through a digital control system.

control counter. The power correction RAM provides a frequency-dependent correction factor which is summed with the user-selected power level. This corrected digital word is sent to the remainder of the power control circuitry via the power control bus.

Power correction factors used in the power correction RAM come from one of two sources. The first is a battery-backed CMOS RAM which stores power level calibration factors for the full bandwidth of the sources. This RAM is write-protected with a user accessible switch. The second source of power correction factors is also a battery-backed CMOS RAM. It contains either 256 or 512 corrections (the choice is determined by the operator) for a specified frequency range. This set of correction factors is used for precision leveling.

Power Level Calibration

Power level calibration involves the first of the two sources of power correction factors. Sources are supplied with power calibrated at the front panel RF port. Power level calibration may also be done in the field. The test equipment required is a 10 dB pad and a power meter with a 0-1 volt full scale reference output. The source and the test equipment are connected as shown in Figure 3. During the power level calibration procedure, one correction factor is stored in the RAM for each 20 MHz over the entire frequency range of the source. For unleveled power output, +15 dBm power output may be specified and the source will deliver the maximum power available.

Figures 4 and 5 show the leveled and unleveled power outputs from a 1-18.6 GHz source. Figure 5 shows output power with the leveling attenuator set for minimum attenuation.

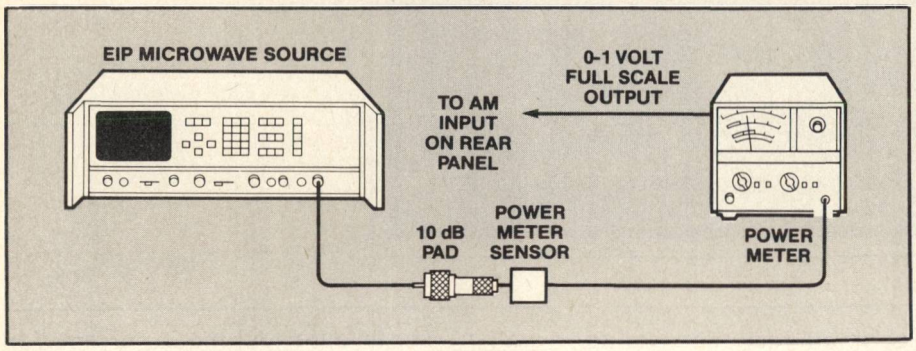


Fig. 3 A simple test equipment configuration for power calibration of the source.

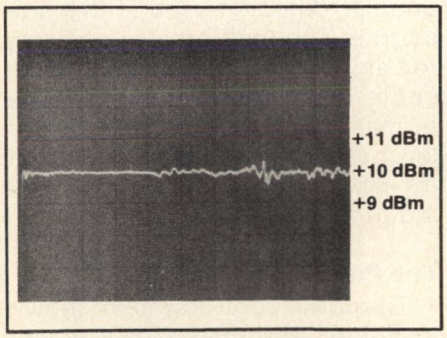


Fig. 4 Power flatness from 1 to 18.6 GHz is within ±0.5 dB.

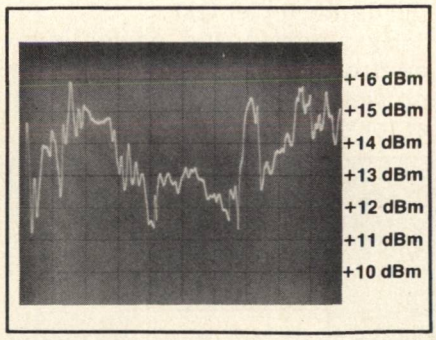


Fig. 5 Maximum power output available between 1 and 18.6 GHz.

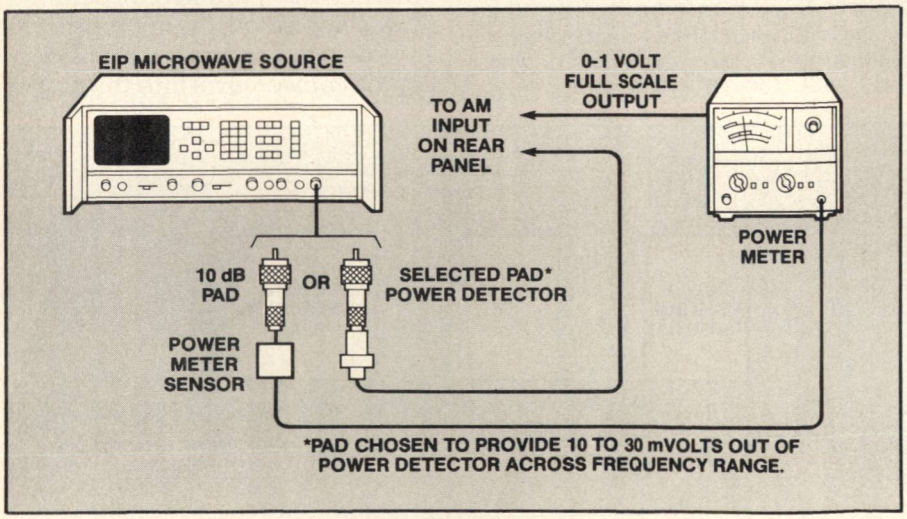


Fig. 6 Two alternative test equipment configurations for precision leveling an EIP Source.

Precision Leveling

Precision leveling permits the user to "customize" a narrow bandwidth (up to 10 GHz wide) for extremely flat power output. It applies only to the frequency sweep and CW modes of operation. For precision leveling, the source is leveled with a crystal detector and appropriate pad or a power meter and 10 dB pad as used for power calibration (see Figure 6). If the source is to be leveled with a crystal detector, a power meter is used first to set an accurate reference power level.

To precision level, the desired frequency range and the number of power corrections points (256 or 512) are selected. The desired

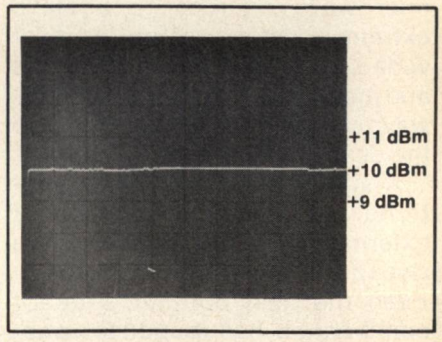


Fig. 7 Precision leveling typically results in power flatness better than +0.05 dB.

leveled output power is set with the power meter and the power meter or crystal detector/pad combination is used to complete the precision leveling process. Figure 7 is a network analyzer display of the 5.9 to 6.4 GHz band leveled at +10 dBm with 256 correction points. The practical limitation on spacing between correction points for precision leveling is 1 MHz, the smallest source frequency increment.

An attempt to use modes other than sweep or CW, or to specify a frequency outside the original precision leveling range, makes the overall power level calibration factors effective. There is the flexibility to switch between the power calibration and precision power correction factors and both types of power control are available via GPIB control.

Whether the source is operated under manual or GPIB control, typical performance includes power accuracy to within ±0.2 dB over the -2 dBm to +10 dBm range and power flatness with frequency to within ±0.1 dB, 1-8 GHz, and ±0.3 dB, 8-18.6 GHz.

Leveling at the Device Under Test

In production test applications, a sweeper may be dedicated to one test operation and the test apparatus remains constant. Figure 8 shows a simple test station for measuring passive component insertion loss with a network analyzer. A 6 or 10 dB pad is included to ensure a good source match. The source can be power level calibrated or precision leveled (or both) to correct the power level at Point "A." This compensates for frequency response variations in the pad and for cabling loss variations to Point "A." The only power level error remaining is due to differences in the characteristics of the calibration detector and the network analyzer detector.

This small error can be eliminated by using the test configuration shown in Figure 9. The power meter used both to level the source at Point "A" and to measure DUT characteristics at Point "B." While this technique does not provide a visual display, it is particularly suited to GPIB-controlled applications and provides accurate measurements at low cost.

When maximum accuracy, flat power and a visual display are required, the procedure illustrated in Figure 10 may be used. It employs the same detector for precision leveling and network analyzer sensing.

The source leveling techniques described in this note afford the user simplicity in the testing process and significantly better power control than previously available in a broadband microwave source. This results in more repeatable and accurate measurements.

APPENDIX

Stored-Digital Leveling Design Considerations

During power level calibration (see article text) the microprocessor clears the power correction RAM and, at every 20 MHz step over the range of the source,

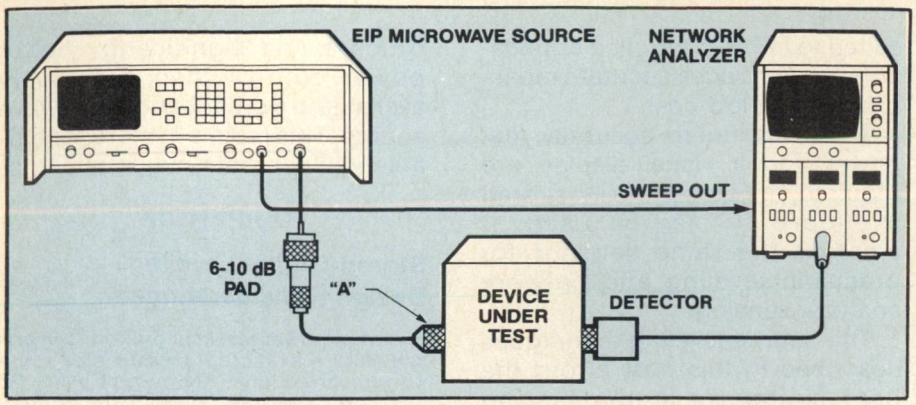


Fig. 8 Leveling the EIP Source at Point "A" results in flat power at the input to the device under test.

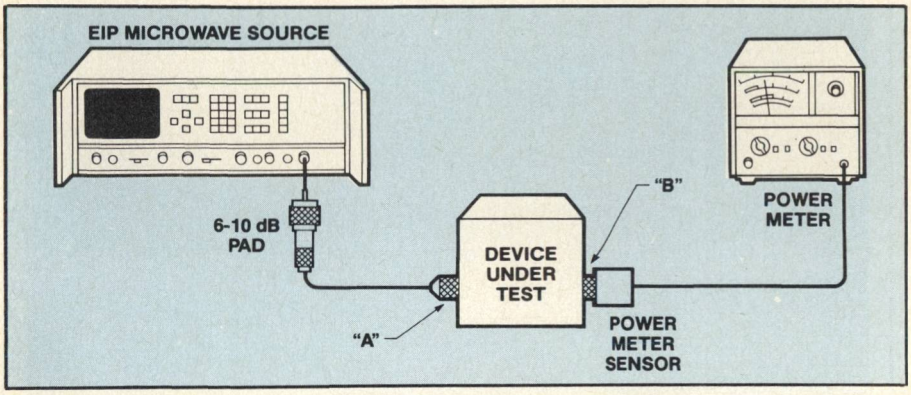


Fig. 9 Leveling and measuring with the same power meter reduces measurement error.

moves the power up/down counter to match the reference power level. The power level is represented by the analog feedback voltage from the power meter or crystal detector. The magnitude and direction (up or down) that the microprocessor must move the power up/down counter is stored in non-volatile memory.

A major objective of the design was to obtain both uniform power output with frequency, and accurate power output. This goal was achieved through the design of the power control system. The design includes a set of PROMs which are used to convert the logarithmic data input to a linear output voltage. This output voltage is the control input to the analog closed-loop leveling system.

The data contained in the PROMs was modified to include the corrections required to match the diode detector's output over the upper end of its dynamic range where the power to voltage conversion changes toward a non-square-law relationship.

Detector corrections included in the PROMs were developed from data measured on many diodes. The stored data is matched to each detector through controls which allow the stored curve to be moved up and down on the actual power output/voltage relationship, thereby ensuring power accuracy.

Another design consideration affecting the leveling operation is the passive role of the 6800 microprocessor during sweep. The microprocessor performs necessary timing calculations and loads various counter and latches prior to the beginning

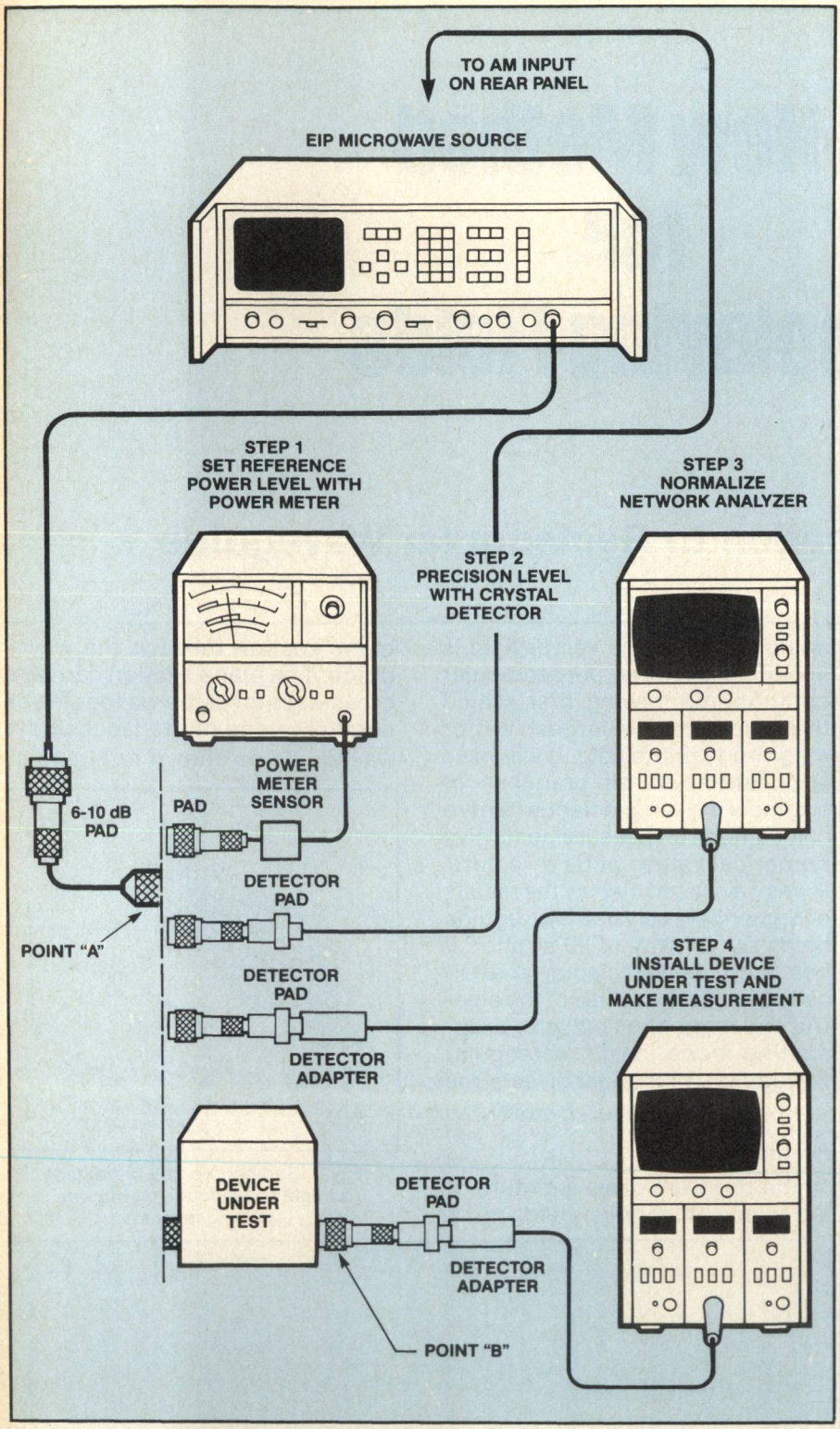


Fig. 10 A four-step process provides leveled power at the input to the device under test and minimizes error when a network analyzer is used.

of each sweep. The microprocessor, however, is not involved in the real-time sweep activity.

The power correction data is stored in a battery-backed CMOS RAM. When the data is to be used, the microprocessor transfers the data to the frequency-bus addressed power correction RAM. Once the data is transferred, the microprocessor is no longer involved in the use of the power correction data.

During both CW and sweep activity, the appropriate bits of the 14-bit digital word corresponding to the active frequency are used as the address for the power correction RAM. Thus, the stored data is automatically transferred to the digital summation used to generate the corrected power control digital word. This word is processed through the conversion PROMs. All of this real-time activity is accomplished without any action by the microprocessor. ■

Technical Note

A New Method for Displaying Fields

and Its Application to Rectangular Waveguide

A. J. Baden Fuller
and
Dr. M. L. X. dos Santos*

A computer program has been written to display the electric and magnetic fields inside rectangular waveguide. It uses analytically calculated values of the field quantities and a newly devised method for the display of 3-D vector fields. We present diagrams of the fields in the waveguide cross-section for selected modes in rectangular waveguide.

Introduction

A computer program has been written to display the electric and magnetic fields for a propagating mode inside rectangular waveguide.[1] It uses a newly devised method for the display of 3-D vector fields.[1,2] An arrow of fixed proportions gives the magnitude and direction of the vector field at each point at which it is known. The arrow head has thickness and the whole arrow is scaled in proportion to the magnitude of the field so that the orientation perpendicular to the plane of the paper is indicated by the body of the head and foreshortening of the image. A computer program has been written to draw such an arrow in the spacially correct position where the vector field is specified by three perpendicular components, having first scaled the arrow to the largest vector magnitude in the field. It will have applications in all branches of engineering and science where calculations or measurements give numerical values of field vectors. It was devised to display the results of numerical analysis of waveguide fields but by way of illustration it has been used to display analytically calculated values of the electric and magnetic fields of a propagating mode inside rectangular waveguide. This paper gives some of the results of that program.

Program

The program gives a picture of the electromagnetic fields in a plane section through the waveguide. The plane section can be a cross-section of the waveguide or parallel to one of the faces of the waveguide as shown in Figure 1.

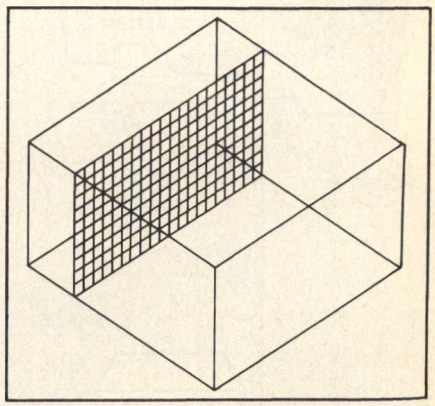


Fig. 1 Geometry of the waveguide sample showing the waveguide cutting planes.

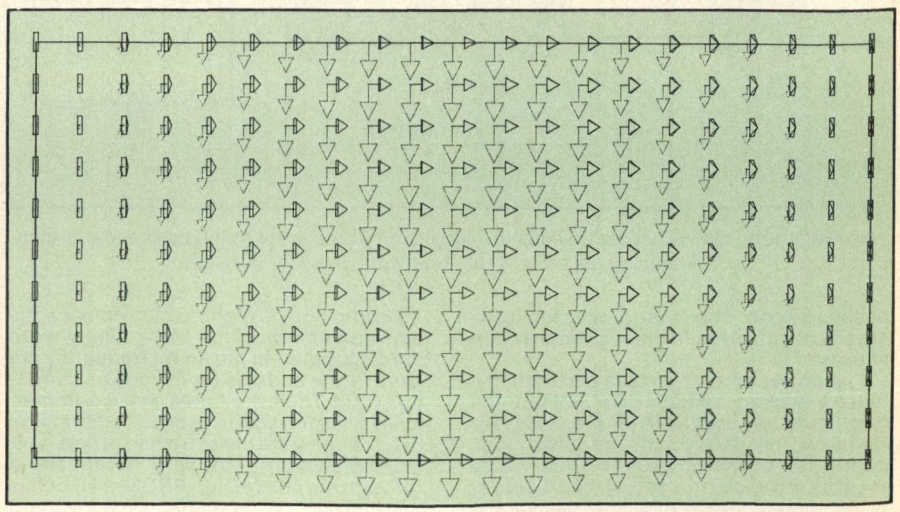


Fig. 2 The electric and magnetic fields of the TE_{10} - mode.

[Continued on page 130]

*Mr. Baden Fuller is at the Department of Engineering, University of Leicester, Leicester, England. Dr. dos Santos is at Pontificia Universidade Catolica, Rio de Janeiro, Brazil.

[From page 128] **A NEW METHOD**

The program divides the plane section into a number of equally spaced nodal points and calculates the waveguide field at every nodal point using the well known analytical expression for the fields in rectangular waveguide.[3] The program needs to be told the dimensions of the cross-section of the rectangular waveguide (ratio b/a) and the plane section where the fields are to be calculated. The number of nodes is chosen by the program according to the dimensions of the waveguide so that the field plot appears reasonable. The program can easily be modified to change the number of nodes; a greater number of nodes will give a diagram having a larger number of arrows with a smaller maximum amplitude. When the values of the field have been calculated, the program divides each field component by the corresponding maximum component found in the plane section so that the maximum field is unity. Then the field values at each point are used to generate the arrow assembly diagram. The arrow drawing routine is a subroutine VECT 3 which has been described elsewhere.[1,2] The program will draw separate diagrams for the electric and magnetic fields or it will draw both fields on the same diagram.

Results

Complete field diagrams in the cross-section of the waveguide for the TE_{10}-, and TM_{21}- modes are shown in Figures 2-3. A short film has also been produced showing the variation with time over two cycles of the fields in the cross-section of the waveguide for the eight modes—TE_{10}, TE_{11}, TE_{20}, TE_{21}, TE_{22}, TM_{11}, TM_{21}, and TM_{22}.

Appendix

Program REWF — REctangular Waveguide Field display.
Language Fortran IV

In its interactive form it is possible, by means of the keyboard, for the operator to specify the display plane, displaying either the magnetic field, the electric field or both together.

It makes use of a more general arrow drawing subroutine, VECT 3, described in Ref. 2. The subroutine, VECT 3, makes use of either the GINO-F graphics package (when it is used interactively) or the GHOST graphics package. It could easily be modified to use alternative basic plotting routines.

The output can be displayed on any graphics device of reasonable resolution. An acceptable image has been produced on a cathode-ray-tube display as well as on a plotter.

On a PDP 11/45 the program, which is overlaid, occupies an area of 30K (16-bit) words. The calculations for Figure 3 were completed in less than one second.

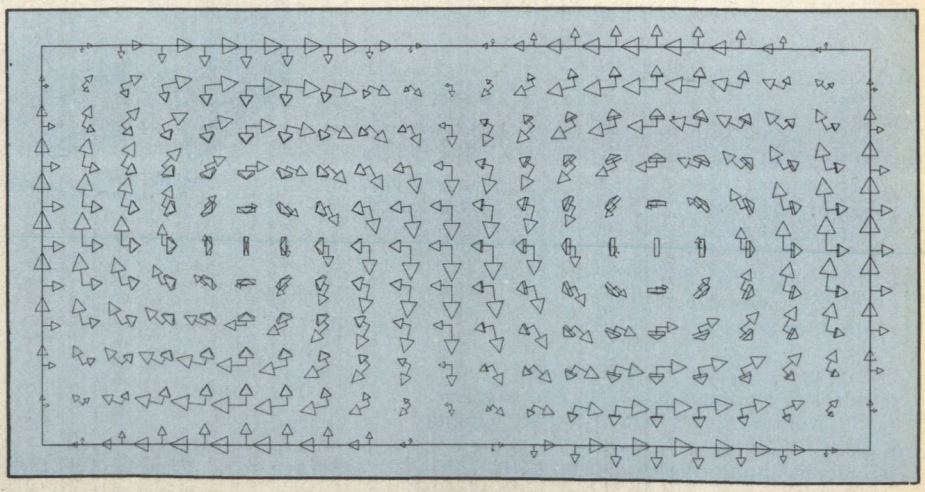


Fig. 3 The magnetic and electric fields of the TM_{21} - mode.

REFERENCES

1. dos Santos, M. L. X., "The Computation of Waveguide Vector Fields and the Generation of Field Patterns Using Computer Graphics," Ph.D. thesis, 1979, University of Leicester, England, Chapter 4.
2. Baden Fuller, A. J., and dos Santos, M. L. X., "Computer Generated Display of 3-D Vector Fields," *Computer-Aided Design.* Vol. 12, pp. 61-66, March 1980.
3. See for example: Collin, R. E.: *Foundations for Microwave Engineering,* Chapter 2. McGraw-Hill, 1966. ■

Digitally Tuned PROM-Corrected VCO

Watkins Johnson
Palo Alto, CA

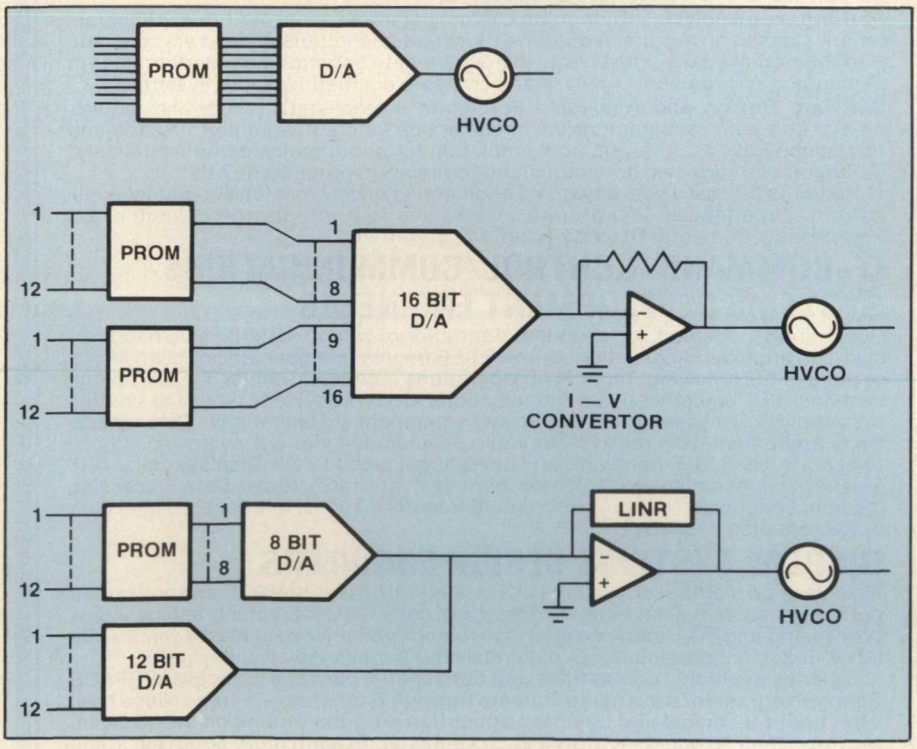
Modern EW systems require microwave sources that can be accurately and rapidly tuned to frequencies up to an octave apart. Until now, the system designer was forced to choose between a wideband YIG oscillator which had the requisite frequency coverage and tuning linearity, but was relatively slow, and VCO's which tune rapidly with excellent set-on accuracy but did not have tuning linearity better than ± ½ percent.

A new generation of digitally tuned and PROM-corrected varactor-controlled oscillators now provides tuning linearity of ± .02% while achieving tuning set-on times of under 200ns. These oscillators utilize a programmable read-only memory (PROM) to store a corrected digital encoding of the frequency command. A simplified block diagram of one of these oscillators is shown in Figure 1 with two different implementations of the PROM correction.

The top block diagram shows the basic concept of the digitally corrected oscillator. A command word is presented to the PROM which in turn outputs the corresponding required digital word to a digital-to-analog convertor. The output of the digital-to-analog convertor (DAC) tunes the RF oscillator.

The second block diagram utilizes two PROMS to convert the 12-bit tuning input word to a 16-bit corrected word. This corrected word is then converted by a 16-bit DAC to tune the RF oscillator. This design yields the greater linearity but is limited in speed by the 16-bit DAC.

The third block diagram utilizes one PROM to convert the 12-bit input word to an eight-bit correction word which is then summed with the output of the directly



Simplified block diagram.

TABLE I

Implementation	Frequency Range (GHz)	Minimum Power Output (dBm)	Settling Time (±4 MHz)	Linearity at Room Temp.	Size
16 Bit	2.6 - 5.2	+12	300 ns	±.02%	2"x2"x2.5"
12 Bit + 8 Bit	6.2 - 12.7	+12	200 ns	±.04%	1.5"x3"x4"

[Continued on page 132]

[from page 131] **VCO**

tuned 12-bit DAC in the operational amplifier current to voltage convertor. This design sometimes requires the use of an analog linearizer to coarsely linearize the tuning characteristics of the RF oscillator. In addition, the linearity is not as good as the 16-bit implementation. The tuning speed, however, is faster because the 16-bit DAC has been replaced with a faster 12-bit DAC.

Both implementations were selected to ensure that a least significant bit change in the input tuning word will always cause a positive, non-zero change in frequency. A simple 12-bit input word converted to a 12-bit corrected word will have portions of the band where a least significant bit change in tuning input will cause no change in output frequency. Some system designs cannot tolerate this.

Typical specifications for the two implementations are given in Table 1. Similar designs can be implemented using different oscillators to obtain octave or greater coverage from 0.5 to 20 GHz. Thin-film microstrip construction is used throughout the unit for all subassemblies. Internal hybrid voltage regulating and temperature-regulating circuitry insure stable outputs with varying bias voltages and ambient temperatures.

Thin-film buffer amplifiers are used to minimize frequency variation with changing load impedances and to provide output power leveling.

Hyperabrupt varactor thin-film oscillators are used to reduce the tuning voltage range to within the range of the operational amplifier current to voltage convertor. These hyperabrupt varactors are specially selected to minimize post-tuning drift.

Present designs use bipolar, fusible line PROMs for correction. Under development are units using electronically erasable PROMs (EE PROMs). These units will allow the system to periodically recalibrate the unit by erasing and resetting the PROMs immediately prior to use, eliminating temperature drift and aging frequency inaccuracies. ■

Comments on 'Calculator Program for Impedance Matching'

J.R.M. Vaughan
Chief Scientist
Litton Industries
Electron Tube Division

The matching section computer program by W.J. Remillard (Microwave Journal, August) sets up a dividing line between real and imaginary solutions which is mathematically correct, but from a practical standpoint may cause adequately good solutions to be rejected because they are not perfect. A solution which is right on the dividing line may be perceived as being "on the ragged edge," and hence to be avoided, when in fact it may be a good design-center solution. A simple example will make this clear: suppose we have a 25 ohm resistive load to match to a 100 ohm line. We know, without any computer program at all, that the solution is a quarter-wave section of 50 ohm line adjacent to the load, and that the exactness of the 50 ohms is not critical; but the program tells us that while 49.999 ohms is acceptable, 50.001 ohms is in the "no solution' region, implying that we should back off from 50 ohms towards a lower value, in order to have a margin of safety.

Now this example is so simple that we are not likely to be misled; but suppose that the load resistance is 22 ohms, which ideally requires a 46.9 ohm matching section — a value not likely to be as readily available as 50 ohm line. Can we use the available 50 ohm line? The program says no, but analysis using a TI-59 program which transforms the impedances over arbitrary line lengths, shows that the bandwidth for, say, 1.5 VSWR is only slightly less than would be obtained with the ideal 46.9 ohm line, as shown in Figure 1. The Remillard program has rejected this solution only because the band center match is not perfect, disregarding the fact that our interest is usually not in a perfect match at a single frequency, but in limiting the mismatch over some finite bandwidth. The hard boundary which the program imposes is really a fuzzy region in which solutions change gradually from good to poor.

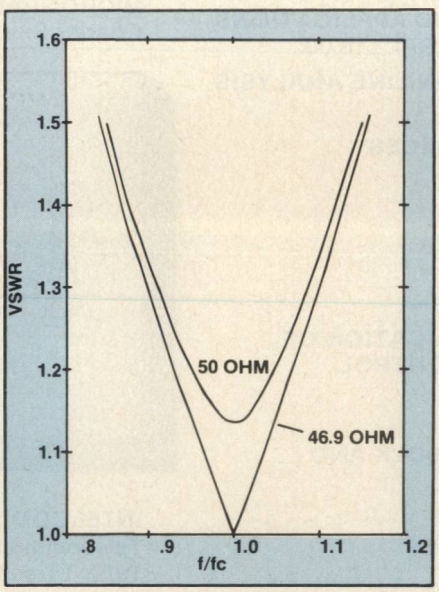


Fig. 1 Comparison of 46.9 and 50 Ohm matching sections — VSWR vs. f/f_c, where f_c is the frequency at which the section is quarterwave. Line = 100 Ohm. Load = 22 + j0 Ohm.

My recommendation is that users modify the program to eliminate the 'stop' when B (step 93) is negative: the program will then keep going for either sign of B; if it is negative, the 'negative square root' will be replaced with the positive, and the flag will be set, causing the calculator to go into the flashing mode (or to print question marks after the values if the printer is in use). The modification is most easily done by changing steps 95 thru 97 to 'Nop' (no operation).

In use, then, an unblinking answer can be accepted as correct but a flashing one, while suspect, may still be useful and should be investigated in more detail, specially if it has advantages such as use of a readily-available line. One should be prepared to modify a flashing solution: if L_1 is just under half a wavelength, move back a half wavelength (which would give a negative value) and then round it off to zero; if L_2 is nearly a quarter wavelength, make it exactly so; but if the values given are far from half or quarter wave, then the case probably is too far from the ideal to be usable. ■

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Erratum

The Appendix to "Passive Direction Finding and Signal Location", *Microwave Journal*, Sept. 1982, pp. 59-76, is reprinted with corrections and additional explanatory material.

APPENDIX

Amplitude comparison measurement is based on the ratio, C, of the signal level received by antenna 2 relative to antenna 1.

$$C = \text{Log}\ \frac{G_2(\theta_2)}{G_1(\theta_1)} \qquad (1)$$

$G_n(\theta_n)$ is gain of antenna n at angle θ_n from boresight.

The measured DF angle is given by:

$$B = \frac{\theta^2_{BW}\ C}{48.1\ (S/2)} \qquad (2)$$

where

θ_{BW} = Beamwidth of the Antenna in Degrees
C = Amplitude Comparison Ratio in dB
S = Squint Angle in Degrees

DF accuracy (ΔB) is

$$\Delta B = \frac{\theta^2_{BW}\ \Delta C}{48.1\ (S/2)} \qquad (3)$$

If $S = \theta_{BW}$ then the DF accuracy reduces to

$$\Delta B = \frac{\theta^2_{BW}\ \Delta C}{24.05} \qquad (4)$$

The single channel amplitude error due to receiver noise is given by

$$\Delta A = \frac{6.14\text{dB}}{\sqrt{\text{SNR}}} \qquad (5)$$

The phase interferometer equation is

$$\phi = \frac{360\ d}{\lambda} \sin\theta \qquad (6)$$

where

ϕ is phase difference between signals received at each antenna
d is antenna spacing
θ is angle of arrival of signal
λ is wavelength of signal

The unambiguous field of view, θ_u, of the two element interferometer is

$$\theta_u = 2 \sin^{-1} \left\{ \frac{\lambda}{2d} \right\} \qquad (7)$$

The spatial angular error, $\Delta\theta$, as a function of the electrical phase error, $\Delta\phi$, is readily derived by differentiating equation 6 to obtain:

$$\Delta\phi = \frac{\Delta\phi}{(360d/\lambda)\ (\cos\theta)} = \frac{\Delta\phi}{360\ df}\ \frac{c}{\cos\theta} \qquad (8)$$

where

$\Delta\theta$ = spatial angular error
$\Delta\phi$ = electrical phase error
θ = spatial angle of arrival
d = end element spacing
f = frequency
c = speed of light

The included angular error due to inaccuracy in the signal frequency measurement is:

$$\text{Error}_{(\text{Degrees})} = \frac{(\Delta f)}{f}\ 57.3\ \tan\theta \qquad (9)$$

Δf = frequency error
f = frequency
θ = angle of signal arrival

An Az/EL system defines a ground emitter position by measuring the azimuth angle of arrival, θ, the elevation angle of arrival, ϕ, and the aircraft altitude, h, with respect to the emitter.

The Slant Range is given by

$$\text{Slant Range } R = \frac{h}{\sin\phi} \qquad (10)$$

Percent range accuracy is

$$\frac{\delta R}{R} = \left\{ \left(\frac{\delta h}{h}\right)^2 + \left(\frac{\delta\phi}{\tan\phi}\right)^2 \right\}^{1/2} \qquad (11)$$

where

δh = Altitude Error
$\delta\phi$ = Depression Angle Measurement Error
δR = Slant Range Error
h = Altitude between Platform and Emitter
R = Slant Range
ϕ = Depression Angle

Triangulation Ranging Error σ_R

$$\frac{\delta_R}{R} = \sqrt{\frac{12}{N}}\ \frac{\delta_\theta}{\Delta\theta} \qquad (12)$$

R is nominal range, $\Delta\theta$ is bearing spread, N is number of intercepts and σ_θ is the angular measurement error.

The relationship between the angular measurement error, σ_θ, the nominal emitter bearing, θ_o, and the measurement system's electrical phase error, σ_ϕ, is given by

$$\delta_\theta = \frac{\sigma_\phi \lambda}{2\pi d \cos\theta_o} \qquad (13)$$

Microwave Products

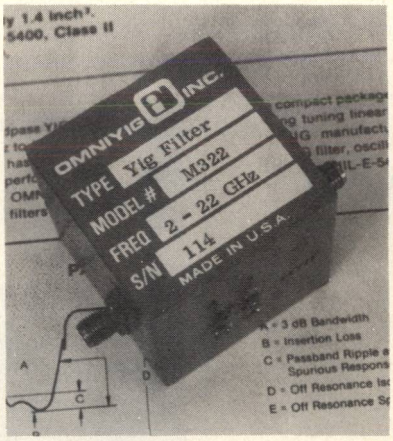
Components

Push-on Subminiature Connectors

The PMMA™ family of coaxial connectors feature a push-on mating face miniaturized to SSMA line size for use in modular system design and other blind mating applications through 18 GHz. The PMMA plug body assembly floats inside a coil spring which is contained in a flanged shell affixed to the package panel. Right angle and flange mounted bodies have a unitized stainless steel machined body. The series includes straight and right angle plugs and jacks for use with both semi-rigid and flexible cables as well as various receptacles. **Automatic Connector Inc., Commack, NY William Pitcher (516) 543-5000.**

Circle 180

2-22 GHz YIG Filter



The Model M322 3-stage YIG filter tunes from 2 - 22 GHz with a 3 dB bandwidth of 25 to 55 MHz. Insertion loss for the unit is less than 4 dB and off-resonance isolation is 60 dB minimum. Size; 1.7 in.^{3}. Integrated drivers are available. **Omniyig Inc., Santa Clara, CA (408) 988-0843.**

Circle 178

75 ohm Right Angle Connector

The 51-128-1195 positive-locking right angle cable plug provides straight-in, straight-out blind mating. Impedance of the connector is 75 ohms and it is designed for use with RG-180/V or RG-195/V cables. A locking ring performs the mating function which is not affected by the weight or pulling of the cable. **Sealectro Corp., RF Components Div., Mamaroneck, NY (914) 698-5600.**

Circle 177

TO-8 Microwave Mixer

The model MC14T hermetically sealed TO-8 mixer covers the RF range of 2.5-3.5 GHz, and the LO range of 1.6-4.4 GHz. The mixer features an IF bandwidth up to 900 MHz with typical conversion loss of 5.5 dB. Typical L-R isolation is 35 dB and L-I isolation is 22 dB at a nominal LO drive of +10 dBm. Price: $53.00 (1-9). Delivery: 2-4 wks. **Magnum Microwave Corp., Sunnyvale, CA David Fealkoff (408) 738-0060.**

Circle 147

HF/VHF Antenna Multicoupler

The Model MDP-2 antenna multicoupler operates over the 5 - 500 MHz range driving eight 50 ohm loads from one signal source. A noise figure of 5.5 dB and signal handling capability of +9 dBm at the input port provide wide dynamic range. Typical SWR is 1.3 input, 1.2 output. Isolation is 50 dB minimum. Typical overall gain to each output is 2 dB. Operating temperature range is 0 - 50°C. N or BNC connectors are available. The unit mounts in a 19" rack and is 3-1/2" high. Price: $1,500.00. Delivery: 90 days. **Mu-Del Electronics, Inc., Silver Spring, MD Irv Kuzminsky (301) 587-6087.**

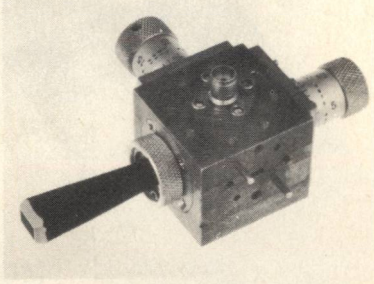
Circle 175

RF and Microwave Switch Drivers

The DS-02, DS-07 and DS-011 hybrid switch drivers switch the bias current of RF and microwave PIN diode switches and attentuators. The units come in inverting and/or non-inverting models with switching speeds from 7 - 10 nS. max. and are TTL compatible. Drivers are manufactured using thick film techniques and meet MIL-STD-883. **Alpha Industries, Inc., Microelectronics Div., Colmar, PA (215) 822-1311.**

Circle 141

220 GHz Frequency Tripler



The model MU3W14-01 frequency tripler using a Schottky varactor diode provides a source of power in the 210 - 230 GHz frequency range. Minimum output is 2 mW, multiplication efficiency (for 15 mW input) is 5% and instantaneous output bandwidth is 3 GHz. Maximum pump power is 40 mW. Input waveguide is WR12, output waveguide (FXR style flange) WR3 and the unit is supplied with external bias supply requiring +15 VDC. Options include mechanical or fixed tuning pump oscillator. **Millitech Corp., Amherst, MA (413) 256-0291.**

Circle 143